A Belle Pixel Vertex Detector Upgrade: Progress and Plans

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ABSTRACT

Future vertex detection at an upgraded KEK-B Factory, already the highest luminosity collider in the world, will require a detector technology capable of withstanding the increased track densities and larger radiation exposures. Near the beam pipe the current silicon strip detectors have projected occupancies in excess of 100%. Recent advancements in deep sub-micron monolithic active pixel sensors look very promising to address this problem. In the context of an upgrade to the Belle vertex detector, the major obstacles to realizing such a device have been concerns about radiation hardness and readout speed. Two prototypes implemented in the TSMC 0.35μm process were developed to address these issues and test results are presented herein. Given the success of these initial prototypes, design concept studies and plans for the next stages of R&D toward a full-sized Pixel Vertex Detector (PVD) are presented. This document is intended as a repository of information and to serve as the basis of a Technical Design Report for a PVD 1.0 system.

Keywords: Active Pixel Sensor, CMOS Monolithic Sensor, vertex detector, radiation hard

1. Introduction

Even prior to the commissioning of the B-Factory detectors, it was realized that improvements in the vertex performance could be made through the adoption of a pixel detector at the innermost tracking layer. Since such an improvement in vertexing was not mandatory for observing CP-violation in the gold-plated $J/\psi\ K_S$ mode, it was not aggressively pursued. Outcomes of these preliminary studies [1] indicated that the two most important aspects to obtaining improvement in a B-Factory environment are moving closer to the interaction point and reducing the amount of material. Therefore the massive hybrid pixel detectors being employed for the LHC are not really viable. As the KEKB machine is the highest luminosity collider in the world, radiation damage close to the interaction point is a major issue. So far CCD-based detectors, so impressively deployed in the SLD experiment and the baseline in a number of linear collider detector concept designs, are very radiation soft despite great efforts to improve their radiation hardness. Meanwhile, great strides have been made recently in applying to vertexing the same active pixel sensor technology that has led to the explosion of CMOS cameras to tracking devices [2]. A pair of prototype devices has been developed in the context of the Super-Belle upgrade and test results and future prospects are described in this note.

2. The Prototype CAP Architecture

There are a number of challenges unique to operation in a B-factory environment. As the electron-positron bunches collide with as little as 2ns separation, the beam is almost DC in terms of timing structure as observed in the detector. Multiple Ampere currents in each beam lead to severe radiation doses for operation close to the beampipe. In contrast with a hadron machine, however, the bulk damage effects are usually negligible. Occupancy of the innermost silicon layer of the current vertex detector is now approximately 10%. Expectations of 20 times higher backgrounds at projected future luminosities will render such a device unusable. Earlier efforts to develop a hybrid pixel detector in the context of lower luminosity operation, based upon bump bonding of a thinned detector with thin readout electronics [3], were abandoned. Based upon experienced gained by other groups and considering the Belle constraints, a variant of the standard Monolithic Active Pixel Sensor (MAPS), denoted the Continuous Acquisition Pixel (CAP), was proposed. The basic CAP concept is quite simple: as a first exercise and to gain some experience with a MAPS detector, we took the standard 3-transistor pixel cell, as illustrated in Figure 1, and built an infrastructure around it to read out as fast as possible.

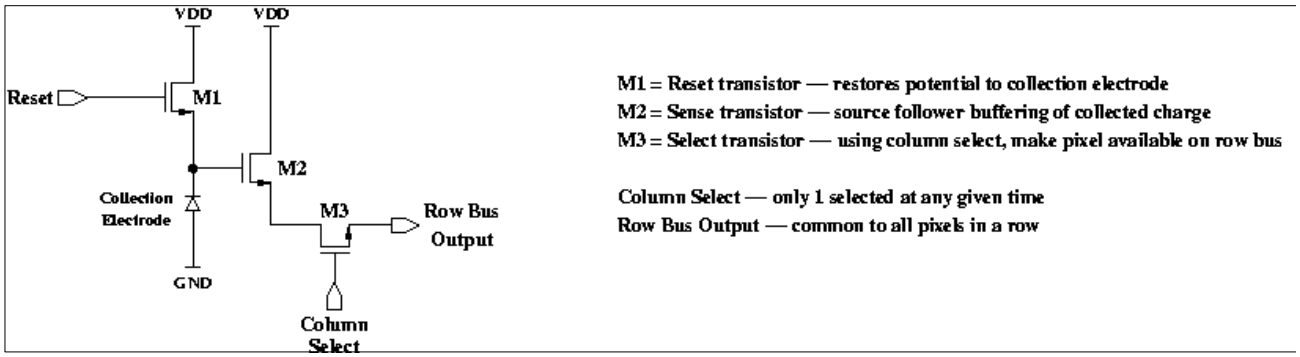

Figure 1: The basic 3-transistor pixel cell. M1 is the reset, M2 senses the gate voltage shift due to collected charge, and M3 is the output select.

As illustrated in the figure above, the basic instrumentation method is very straightforward. An electrode is tied to the gate of transistor M2. When held at a positive potential with respect to the surrounding well and substrate, electrons from deposited ionization are collected on this electrode. As this eventually causes the collection potential to be lost due to negative charging, a periodic reset must be applied to transistor M1 to restore the collection potential. A further transistor, M3, provides the mechanism by which individual pixels may be selectively accessed for readout. There are two important features of this technique. First, as M2 is used as a MOSFET source follower, the miniscule charge on this tiny transistor is never moved anywhere for measurement. This is an important point since with a electrode + gate capacitance on the order of a few femto-Farads, something like 50uV per single electron sensitivity is obtained. A second key element of this tiny charge is that because of the finite charges involved, the actual reset voltage after the application of the M1 transistor reset is uncertain by an amount proportional to a factor of kT (thermal fluctuations) and irreducible. The common method adopted to deal with this is to provide so-called correlated double sampling. In this technique, M2 is sampled immediately after M1 reset. M2 is then subsequently sampled at a later time. The difference between these samples will then be a combination of system noise, leakage current and any deposited ionization. In order to gain experience with this architecture, two variations of this basic theme are presented below. The first, denoted CAP1 consists really only the above mentioned 3 transistor circuit and an array of logic and analog multiplexors to pass the analog values out as promptly as possible.

2.1. The CAP1 Design

The CAP1 design is illustrated in Figure 2, which contains a photograph of the actual layout. CAP1 consists of an array of 6336 basic 3-transistor pixels, some mechanism to shift a token from column to column for readout, and some output multiplexors and amplifiers. Input pads drive the control signals from the Front-End board to the CAP1. 12 output pads drive the analog signals. A powerful and simple test feature is provided by a "Calibrate" test pad, which allows the sense transistor of a test pixel to be set to a determined level. This feature is very useful for gain calibration and for debugging ("frame alignment" in software for example).

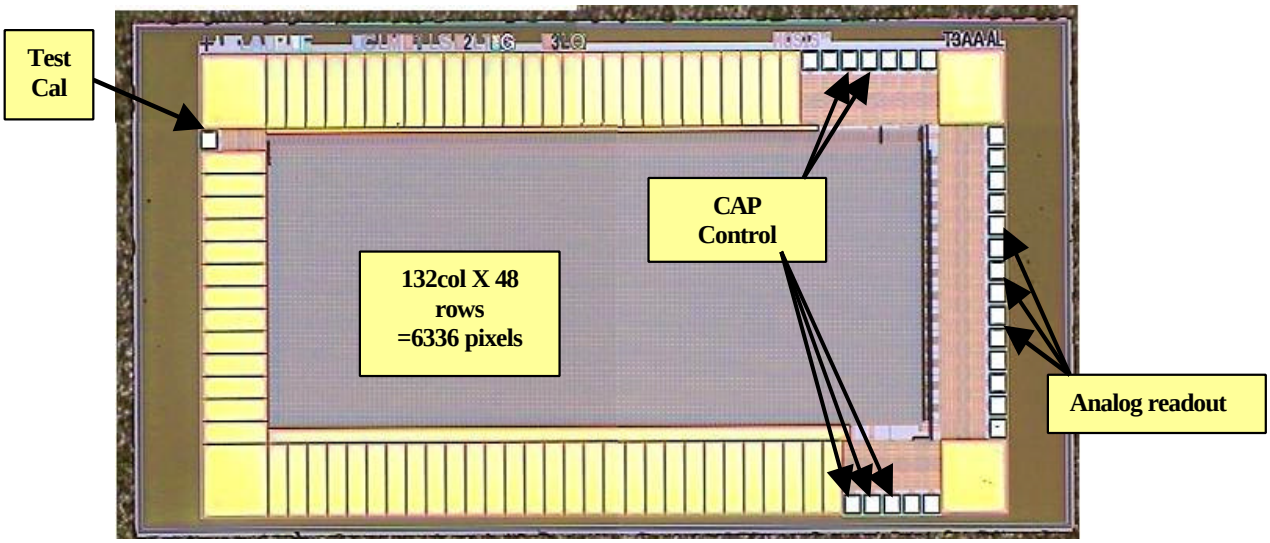

Figure 2: Die photograph and key elements of the CAP1 pixel prototype chip.

Each of these 6336 pixels are 22.5μm square and the sense electrode is approximately 3.6fF capacitance collectively. This choice was dictated by the desire to do a 4:1 analog multiplex on the output row for a 90μm output wire bonding pad pitch. With a thought toward making the device thin, the only place in this circuit that draws significant power is along the right periphery, representing a portion of the circuit outside the tracking acceptance and mounted to a massive thermal heat sink. Column select logic along the top requires approximately 90μm of vertical space and is independent of the height of the die. Note that due to cost constraints, wire bonding pads have been wrapped around from the right edge to top and bottom. Also, in order to speed the layout and provide robustness to this first iteration, a full ESD protection has been utilized. In the full-sized detector (CAP3), the fill factor will be improved greatly.

Readout speed in these first two designs, CAP1 and CAP2, is expected to be somewhat limited by the settling time of a given pixel in driving the long row bus lines. Additional settling time is required for the output of the analog buffer amplifiers driving potentially large external capacitance.

2.2. The CAP2 Design

The basic design of CAP1 is quite simplistic and probably does not have sufficient frame rate to handle the occupancy of the Super-Belle vertex interaction region. For the design of CAP2, 8 storage buffers were implemented in each pixel cell, as well as a mechanism to loop through the storage buffers and select the appropriate one (for read and write). Hence in CAP2, data can be recorded in each pixel for the trigger latency time, and do not need to be transferred out of the CAP in real time: only the relevant data frames - corresponding to a trigger- needs to be broadcasted. Figure 3 shows the schematic and the layout of a pixel cell in CAP2, corresponding to an area 22.5μm on a side.

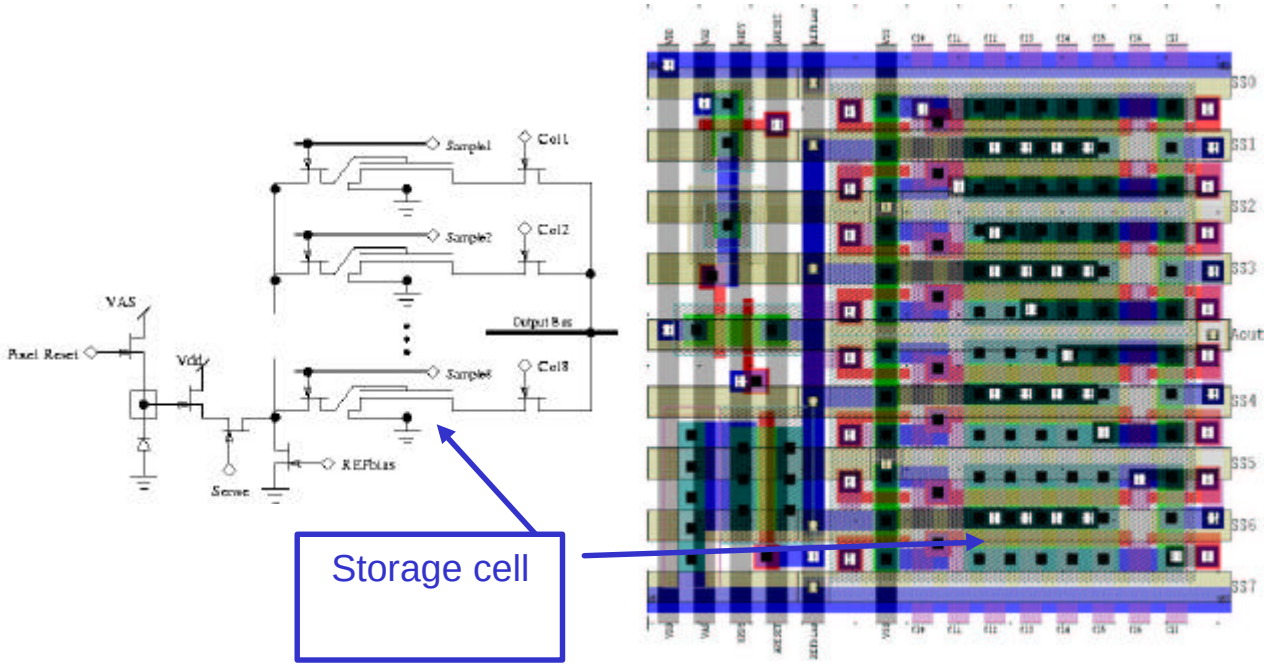

Figure 3: Schematic (left) and layout (right) of a CAP2 pixel. In the 0.35μm process chosen, eight storage cells are available for each pixel with decoupled write and read selects.

3. CAP1, CAP2 Readout system

The setup developed to read out CAP1 and CAP2 is, from a hardware point of view, basically the same. It consists of three blocks as shown in Figure 4. In the first inset figure, the CAP1 / CAP2 MAPS in mounted in a chip carrier and is wire-bonded to the chip carrier's bonding pads. In the second inset, the chip carrier itself is mounted onto a Front-End board, denoted as F1 / F2. F1 is the first iteration of this Front-End board, where data is transmitted in analog form (via SMA connector/cable) to a Back-End board (B1). F2 is the second version of the Front-End board developed, where digitalization of the data occurs on the Front-End board and data is than transmitted digitally. Last piece of hardware needed is a Back-End board, which provides an interface between the F1/2 boards and the compact-PCI (cPCI) data acquisition computer. This board is denoted B1/2, where the index denotes the two schemes chosen (either analog transmission from F to B and digitalization on B, or digitalization on F and transmission of digitized data from F to B). Please note also that using a single Back-End board, four CAP + Front-End board assemblies can be read in parallel using one cPCI slot.

The main advantage of doing the digitization on the Front-End board is better control of the noise level in the system. The main inconvenience is the need to then handle a highly populated Front-End board, an increase in the number of data lines from F to B boards, as well as synchronization issues between the Front-End boards. Note finally that the only difference between CAP1 / CAP2 operation lies in the use made of some programmable chips sitting on the Front-End board / Back-End board, as well as changes in the data acquisition software.

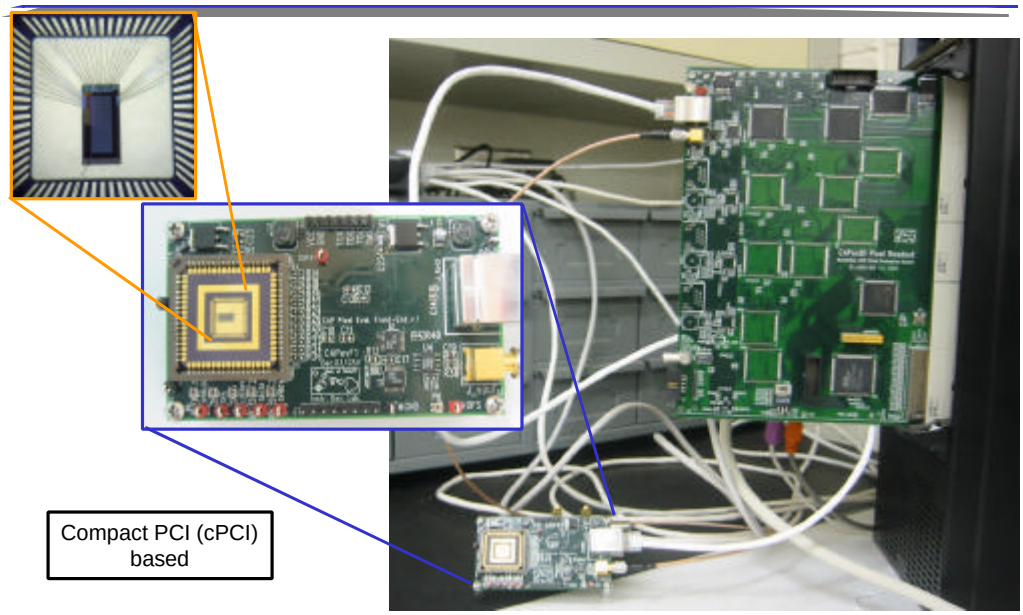

Figure 4: Main components of the CAP1 / CAP2 readout system. A MAPS sensor wire-bonded on a chip carrier can be seen in the top left insert. The Front-End board can be seen in the middle (F1 in the case of this picture). Finally the right picture shows the developed analog version of the Back-End board (B1 here), connected to a single Front-End board through a digital cable and an analog one. Note that for the second version developed (F2 to B2), the digital data are transmitted through two of these standard Category 5 Ethernet cable.

Due to settling time limitations of external amplifiers used, one frame of the CAP1 pixel detector requires about one millisecond for readout. With the need to read two frames -CDS-, and the necessary long charge-integration time related to the fact that there is no analog pipeline buffer in CAP1, we finally operated CAP1 at between about 5 to 10 samples a second. This is somewhat limited by the data processing time, and a desire to maintain an optimal livetime given this processing time. Considering all processing steps, a final CAP1 livetime in "self triggered" mode has been rather (from ~4% to ~30% during our tests). However, a distinct advantage of this operational mode is that no external trigger is required, and given the very low noise trigger rates, in general guarantees that a real signal is present – corresponding to 100% efficiency.

This situation is different with CAP2, as the second iteration of the CAP is externally triggered, and the data internally buffered in every pixel. Thus the "live-time" depends mainly on the choice of sampling frequency and data readout time when a First Level Trigger –L1T- occurs. Extended discussion of the data volume, data readout rate and such can be found in the next section.

4.CAP Prototype Test Results

Far from an exhaustive list, presented below are some of the test results obtained to date, which comprise the key functionality requirements of such a pixel detector to be useful for a Super-Belle vertex upgrade:

- Basic performance – sampling and readout speed consistent with the Super-Belle environment
- Signal to Noise Ratio – sufficient to establish a viable improvement in vertex resolution
- Radiation hardness – capable of surviving and efficient operation at 20Mrad dose
- Intrinsic resolution – maintain with a 40-50μm thin detector

4.1. *Basic performance*

Figure 5 shows graphically the method that is used to extract from the CAP the relevant frame difference data, denoted the Correlated Double Sampling (CDS) method.

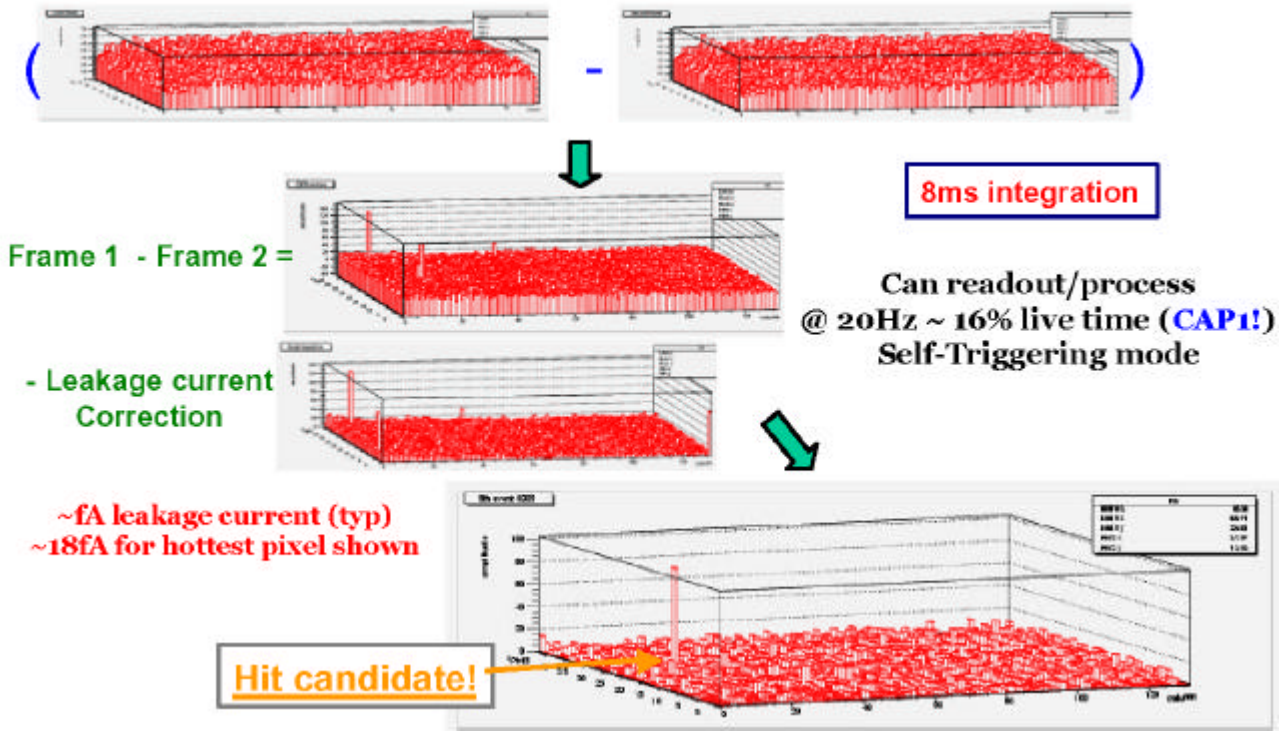

Figure 5: **Illustration of the principle of the Correlated Double Sampling (CDS) method. Due to threshold spread and irreducible uncertainty in the analog reset process of the miniscule capacitance of the sense electrode and transistor, it is necessary to take a difference between a before and after frame bounding the charge deposition event of interest.**

Prior to writing of the data frame difference, the typical leakage current and typical noise of each pixel in the CAP array is extracted. The basic idea of the CDS method is then as follows: a reset is first sent to the pixel, which brings its sense transistor back to a known state modulo electron counting statistics (with respect to the dynamic range of the sense transistor). A first frame (complete pixel array) is acquired, which will give the baseline for the data acquisition. Then the sensor is active for a certain time, which is called the charge integration time. A second complete frame is then acquired. By taking the difference between these two frames and correcting then for leakage current in every pixel, a charge deposition in each pixel is thus recorded. From this process, clear event candidates appear without further signal processing. Such a sample event is seen at the end of this processing chain in Figure 5.

While the leakage current make look dramatic in this figure, even the worst-case leakage corresponds to only 18fA and is a dramatization of the very long integration time chosen for this exposure. For the ~10μs integration periods needed for occupancy reasons for Super-Belle, this level of leakage current is completely negligible. As an archival fact, for completely historical reasons, the first cosmic muon event is readily seen in Figure 6, illustrating that decent signal to noise ration (SNR) was obtained at even very early stages, though some amount of periodic (switching power supply) noise is clearly evident.

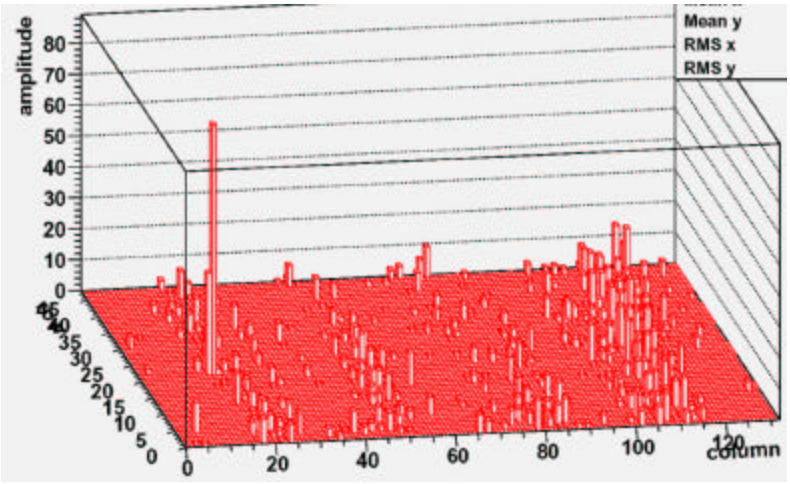

Figure 6: A historical figure demonstrating the first cosmic muon observed by the CAP pixel detector.

4.2. Signal-to-Noise Ratio

Figure 7 illustrates the complete readout chain, from the charge collecting diode to the output of the ADC, with some indicative values of the gain and noise, in the case of a CAP1 operated with F1 / B1. Note that with F2 / B2, and the second scheme chosen where the ADC sits on the Front-End side, the noise level is reduced to ~ 16e-.

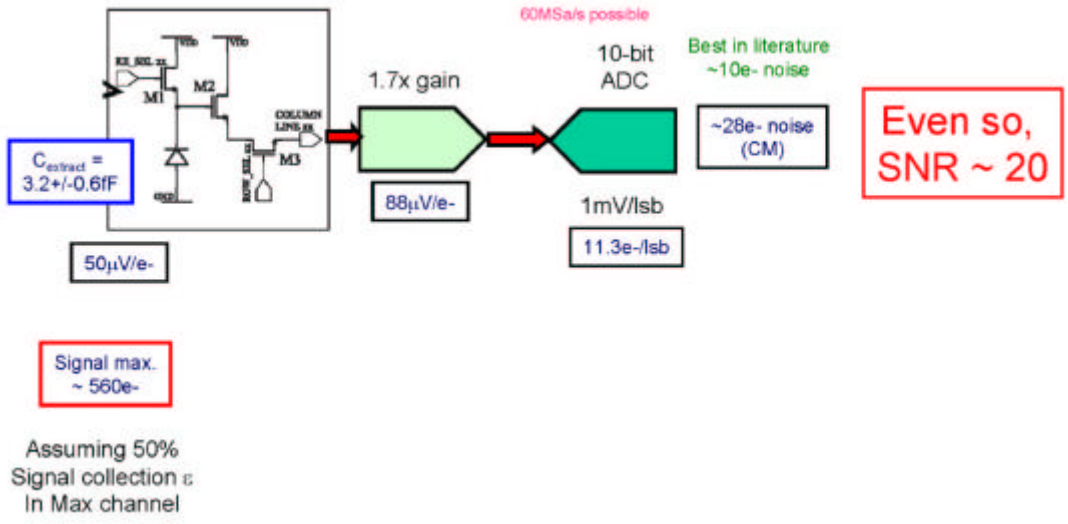

Figure 7: Signal readout chain illustrated with the gain and noise indicated, as measured in CAP1 with F1/B1.

It is then interesting to know how the resolution degrades with respect to noise level in the system. A toy Monte-Carlo was developed containing random hit generation, diffusion simulation (substrate loss, recombination, noise) and reconstructing then the tracks using a "center of gravity" of the cluster of hits.
Figure 8 shows the result of such a simulation, taking a 3 by 3 pixel array and a 5 by 5 one. Two main points should be highlighted: first, it is to be noted that the reconstruction in the 5X5 case is worse than in the 3X3 case, as soon as the noise levels exceed ~5e-. Realistically, we should expect a noise level two to three times

worse, hence we will not gain from doing large clustering. Second, note that the extracted resolution stays below 4μm until close to 30e- of noise in the 3X3 case. The resolution versus noise curve is quite flat over the entire the range studied. The 16e- level point is highlighted in Figure 8, which corresponds to what has been obtained with F2 / B2.

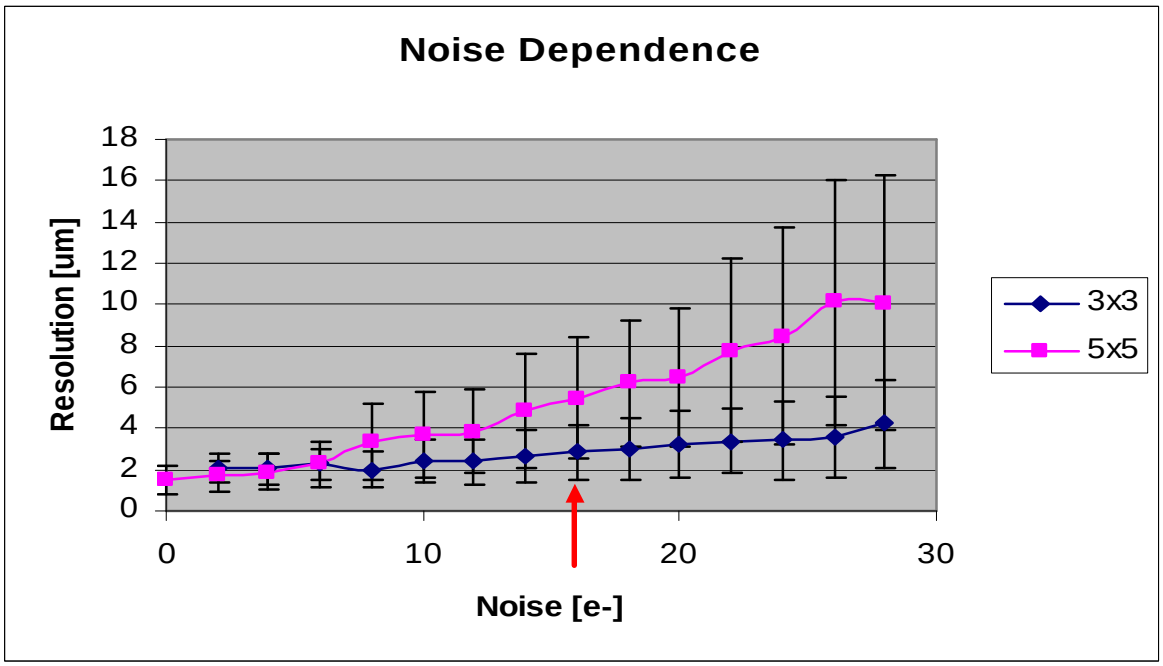

Figure 8: Toy Monte-Carlo; resolution in um as a function of noise (e-). The arrow points to the noise level achieved in the lab in the F2 / B2 case.

4.3. Intrinsic Resolution

An upper limit on the intrinsic resolution was obtained during a beam test performed at KEK in the beginning of June 2004. In this test, an array of four CAP detectors were arranged in the π-2 beam as shown in Figure 9 (not to scale).

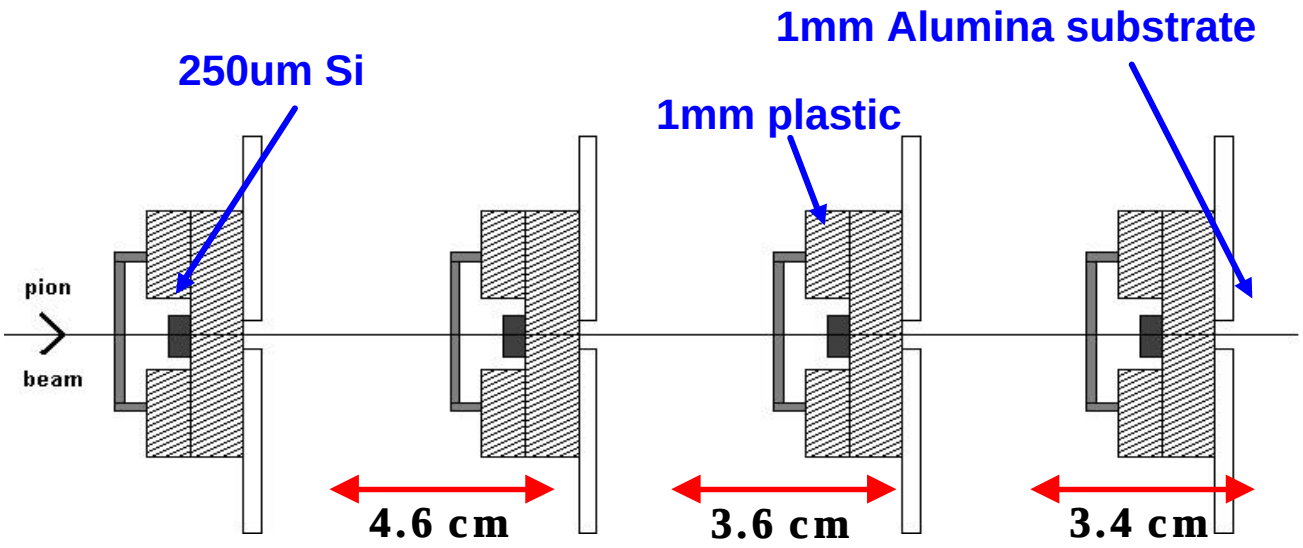

Figure 9: Schematics of the four MAPS in the pion beam with materials -not to scale-. The four MAPS are drawn in black, plastic covers are in gray and the pixel carriers are shaded.

This determination of the intrinsic resolution was limited by a number of constraints; such as the spacing between the detectors, the material budget, and residual misalignment due to limited statistics. It is also highly dependent on the pion momentum. Figure 10 contains the results from a GEANT simulation of our beam test conditions with realistic spacing and material for the detectors.

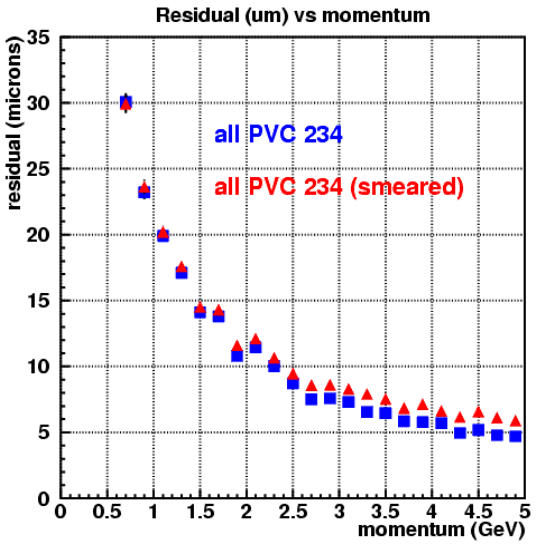

Figure 10: Result of a GEANT simulation of the June 2004 KEK Beamtest, showing the ultimate residual that could be determined (in micrometers) during the first pixel as a function of pion momentum (in GeV/c [sic]).

After a "by hand" alignment procedure, then followed by software-corrected on a partial data sample, we were able to extract an experimental upper limit on the intrinsic resolution close to 11 μm from a second sample of about 2000 4GeV pion tracks, which is shown in Figure 11.

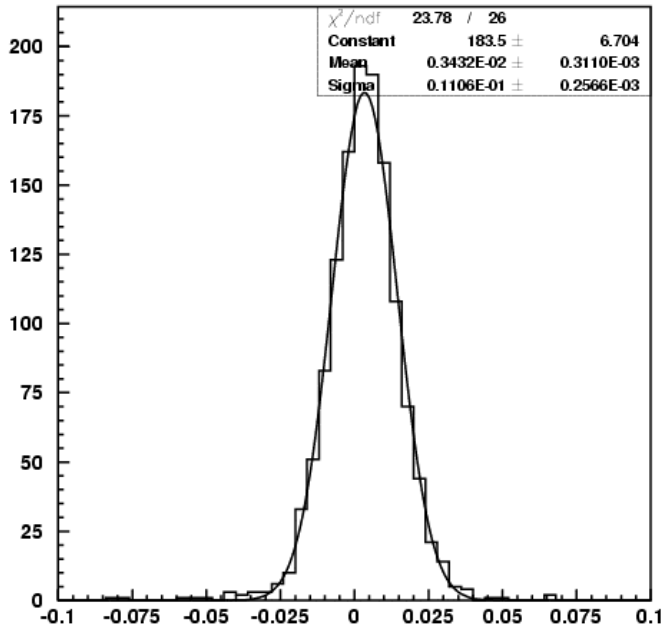

Figure 11: The final residual obtained from data during the first pixel beam test with 4GeV/c pions. On the x-axis, the residual in microns, in y, number of entries in the histogram.

4.4. Charge collection and SNR versus cluster size

Knowledge of the typical charge collection in the pixel array is essential for the development of any clustering algorithm. That is one of the studies pursued during the first beam test. Figure 12 shows the correspondence between the number of pixels used to extract a signal in the pixel array and the signal level, for each of the four detectors used in the setup.

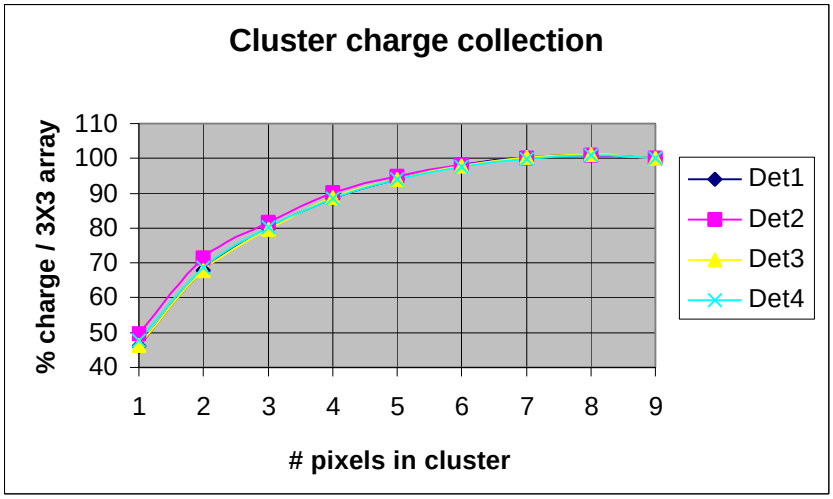

Figure 12: Collected charge as a function of the cluster size (most probable value), from beam test data.

From simulation expectations, we took as a hypothesis that a 3X3 pixel array collects close to the entire charge. When one considers the shape of the curves in Figure 12 (saturation observed for 6/7/8 pixels in the cluster), this seems a reasonable assumption to make. Quantitatively, the peak signal pixel contains about 50% of the total collected charge, while the four main pixels contain about 90% of the charge.

Figure 13 shows a complementary study, where the SNR is now plotted as a function of the number of pixels.

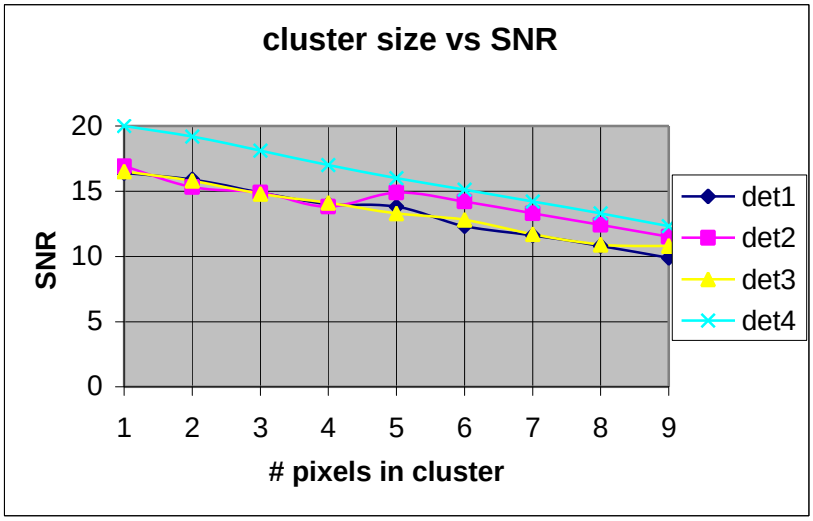

Figure 13: SNR as a function of the cluster size (mean value), from beam test data.

4.5. Radiation Hardness

Irradiation with a ^{60}Co source of numerous devices has been carried out, as illustrated in Figure 14. While the use of "enclosed" transistors [4,5] was not implemented in this design, from previous measurements the threshold voltage shifts of this deep submicron process were determined to be quite acceptable. The following plot compares our measured pixel leakage current values with those reported by Eid *et al*. [6], which have demonstrated survival to 30MRad. In fact the test performed by this group was halted due to time constraints on the irradiator and not any indications of trouble. As may be seen in Figure 14, for dose rates above about 5MRad, the leakage current seems to saturate. Complete annealing of the highest exposures has yet to be completed.

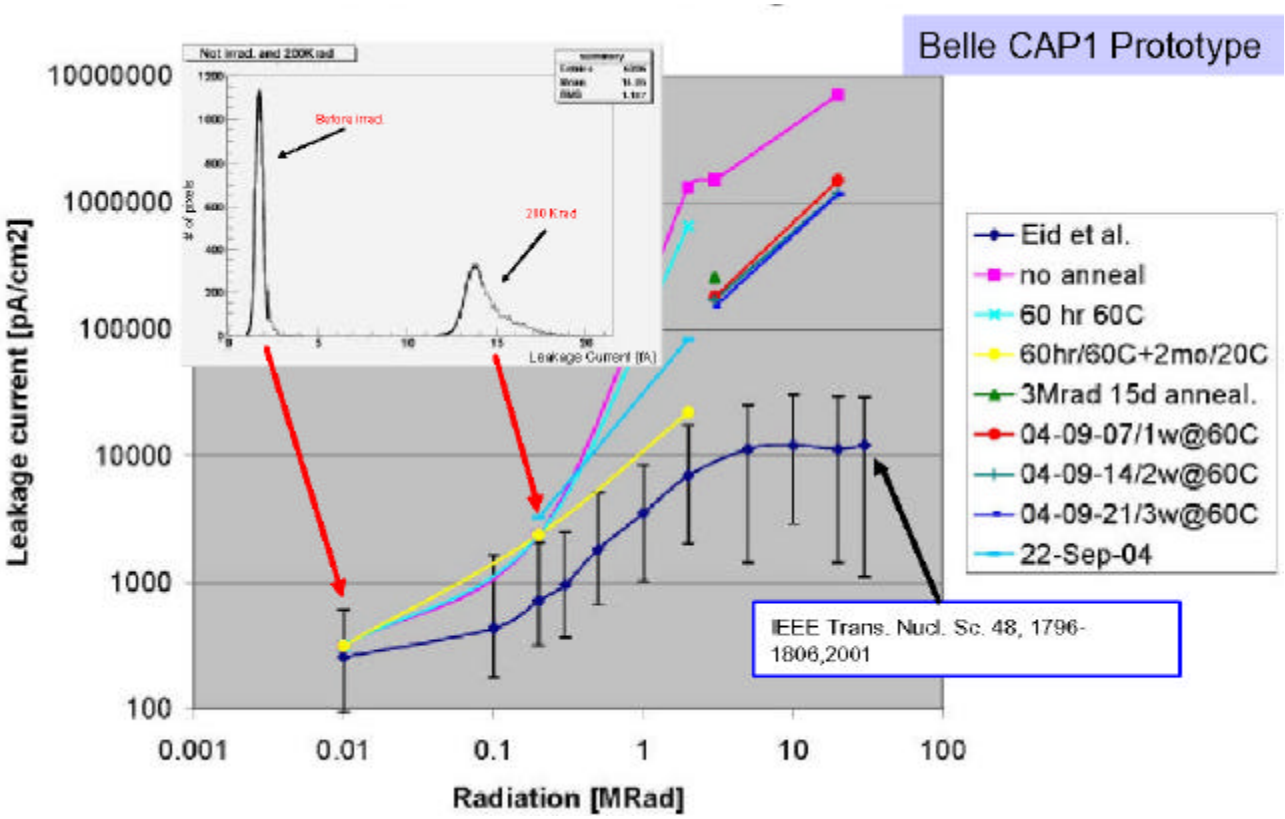

Figure 14: Leakage current as a function of radiation dose. Due to high dose rates, significant reduction is seen with annealing, where Eid et. al [6] is the ideal limiting case.

In addition to increased leakage current, there is concern about decreased charge collection efficiency. This will be explored during an upcoming beam test. Assuming a source times collection efficiency signal peak pixel of 550e-, a study of the SNR versus integration time can be found in Figure 15. At short shaping time, the impact of even large leakage currents is very modest. As long as the charge collection efficiency remains acceptable, operation of this device to 20Mrad or more should be possible.

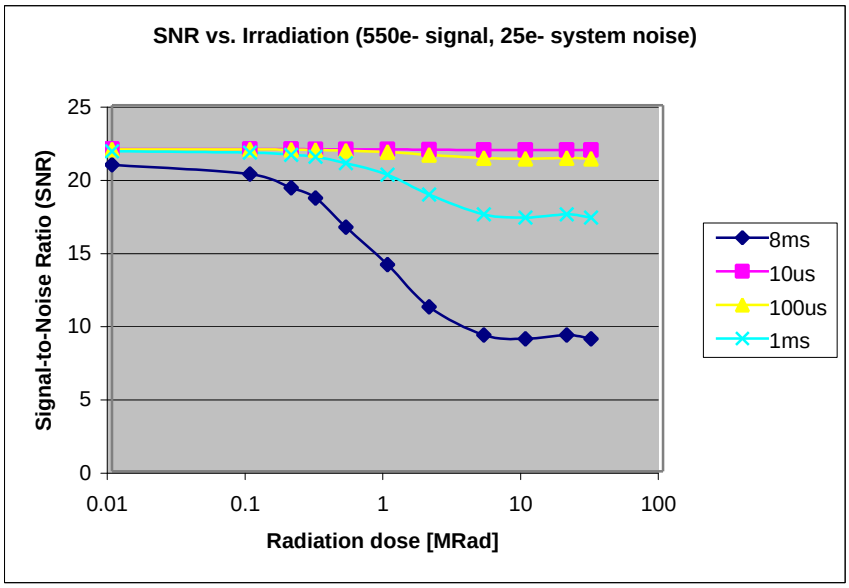

Figure 15: Expected Signal-to-Noise Performance degradation versus leakage current for a number of different integration periods based upon the leakage currents shown in the previous figure.

5.PVD "full-size" Prototypes

In order to assess the system performance of a full-scale pixel readout running at realistic readout speed, a third generation of CAP prototype, designated CAP3, is being fabricated. Above a maximum die size the cost of the fabricated chip increases noticeably, and a hard limit, defined by the maximum standard reticle size, is about ~21mm in a linear dimension. Considering these constraints for CAP3 the pixel array is increased to 928 columns by 128 rows of pixels as seen in Figure 16. This corresponds to ~120k pixels, which is approximately the number of channels in the current SVD2 system. The unit size of the CAP3 MAPS will hence be ~3x21 mm. This is large enough to consider building a first generation Pixel Vertex Detector from these elements. Such a layout may be seen in Figure 17, where the acceptance of a future "compact" beampipe is considered.

Yet, critical to making a practical readout system is the ability to handle the enormous data rates intrinsic to such a finely segmented detector. To do so requires a companion ASIC (PIXRO1) of very high performance.

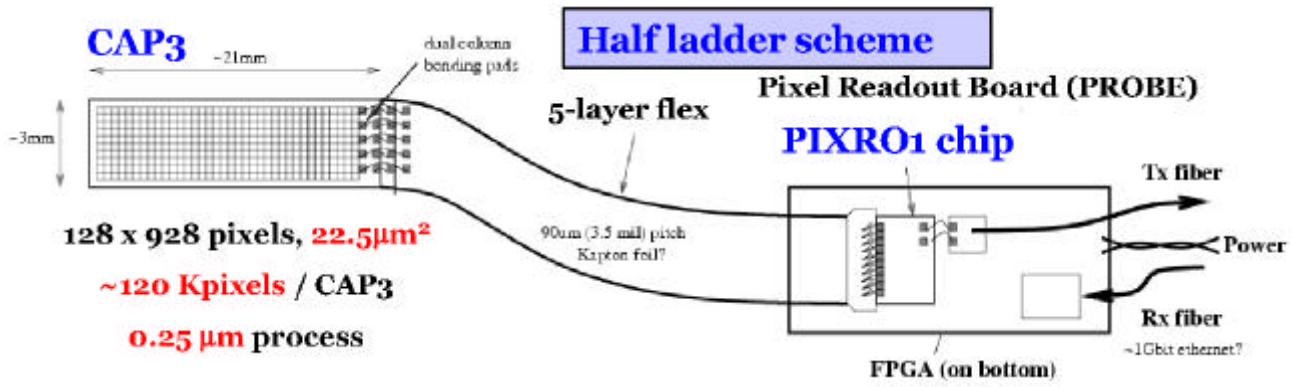

Figure 16: Layout of the "full-sized" detector configuration, which consists of a 120k channel CAP3 sensor (left) and a signal processing ASIC (PIXRO1, at right).

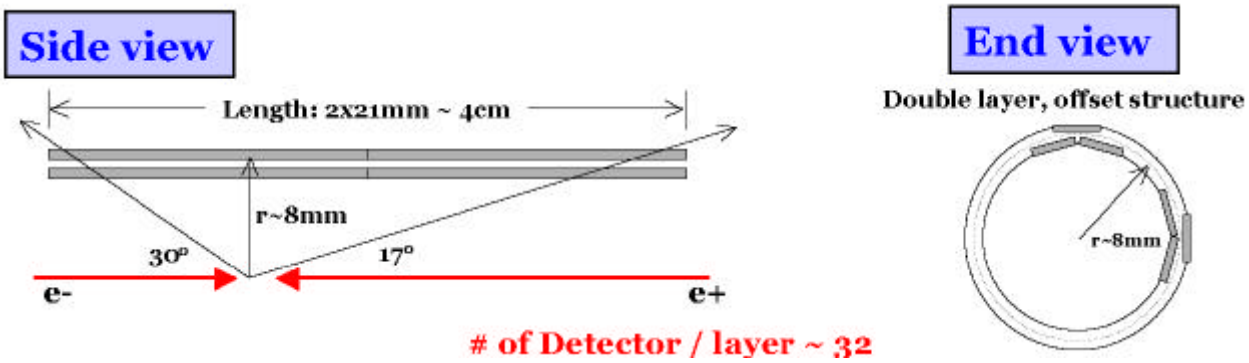

Figure 17 Mechanical configuration of the "ideal" pixel geometry given constraints on die reticle size. This would require a 7mm beampipe radius versus the 10mm currently planned.

It is possible to fashion a ladder from these CAP3 sensors that could be fashioned into an SVD2 innermost layer drop-in. This would permit the possibility of an earlier installation without a redesign of the interaction region. Such a scheme is under consideration and will be presented as part of a future PVD Technical Design Report.

5.1. Prototype System Architecture

A functional overview of the full-size prototype is illustrated in Figure 18. The CAP3 sensor is connected with a flex circuit to a readout card which contains the electronics for signal processing and control. The high-speed signal processing is done within the PIXRO1 chip, which is a SiGe BiCMOS chip capable of very high-speed signal processing. The output data stream is sent via a high-speed fiber optic link to a receiver card, which is to eventually be implemented on a FINESSE card.

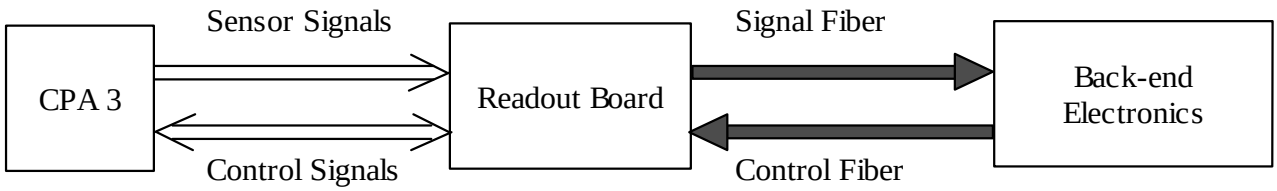

Figure 18: Pixel Detector Basic System Components.

The system diagram of the PVD full-size prototype is shown in Figure 19. The overall scheme for performing the readout has undergone a number of studies and since the final PIXRO1 has not yet been submitted, it is still a work in progress. The general scheme is similar in all cases considered below.

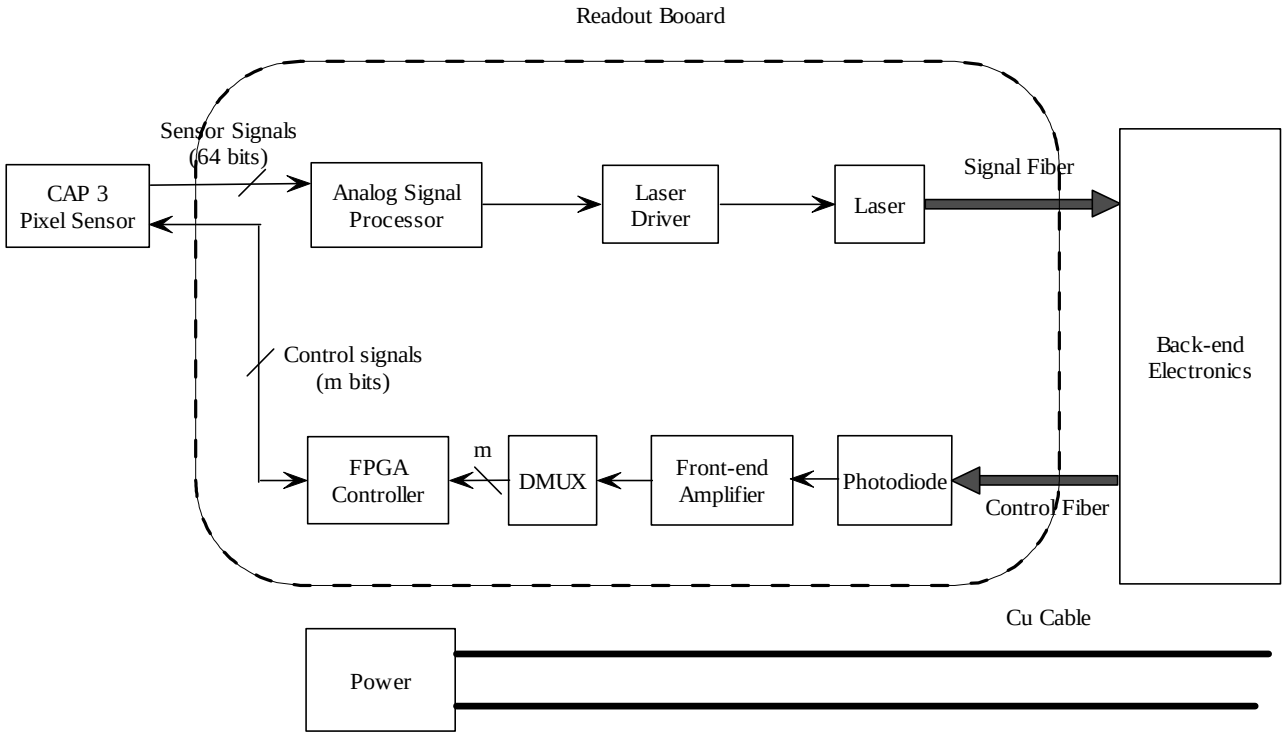

Figure 19: System Diagram of a PVD full-size Prototype.

The specifics of the analog processing functionality of the PIXRO1 chip has been left intentionally blank as it is one of the key R&D items at this time. A series of possible techniques are described in subsequent subsections below. SPICE simulations are also presented.

5.2. CAP3 Architecture

As mentioned above the CAP3 detector consists of an array of 928 columns by 128 rows of pixels, each 22.5μm^2. This corresponds to just under 120k pixels. Inside each pixel is a 5 deep sample pair pipeline. While these could be treated as 10 independent samples, for operational convenience, it is planned to treat them as 5 CDS samples. This then corresponds to separate beam orbits, for instance. As with CAP2 this decoupling of the sampling frequency with the readout frequency allows for a reduction in the data flow required out of the CAP3. At a 10kHz trigger rate, this still corresponds to a throughput of about 1.2Gsample pairs per second. As seen in Figure 16 direct CDS is done by broadcasting signal pairs from the CAP3 to the PIXRO1, which then directly differences them. Thus the 32 signal channels correspond to 16 samples per transfer cycle. To meet the latency requirements, these signals must be transferred at a rate of about 100MHz.

5.3. PIXRO Chip

The PIXRO1 is a readout system for CAP3, which differentiates the analog data acquired in pixel sensor arrays by correlated double sampling, pipelines it into its memories, and then converts it into digital form, finally sending the data through a laser driver.

As mentioned above, there are 32 channels from CAP3. The aim of the project is to use the IBM 0.5um SiGe BiCMOS 5HP process offered by MOSIS to achieve a 100μs readout speed. The consideration of low power is not included so far.

There are four schemes, and could might be more, for this design. The reason for the variety is that different approaches have their own advantages and disadvantages. Additionally, there will be variance between theory and application. A priori, it is difficult to predict which scheme will be best and simulation studies of these techniques are valuable in this determination. In terms of deciding which to consider prototyping, the simplest possible scheme which meets the requirements is best.

5.3.1. PIXRO1 Method 1: High-speed Analog Multiplexer

A pure analog processing method is considered in Method 1. As illustrated in Figure 20, 32 differential outputs from CAP3, are fed into individual sample and hold cells. Each signal is held for some period, and then is transferred to the output of the analog MUX. Thus, the analog MUX, which is composed of several serried stages of two-bit analog multiplexers, converts the parallel signals into series signals. The buffer amplifier enhances the linearity, and then the signals are put into a laser driver.

Its advantage is that it avoids using ADC at the near end. Thus, high performance ADC can be used. In addition, the sample and hold cell is a simple analog memory system. The disadvantage is the analog signal from the laser driver is not that well characterized, and might be subject to long term voltage drift and noise.

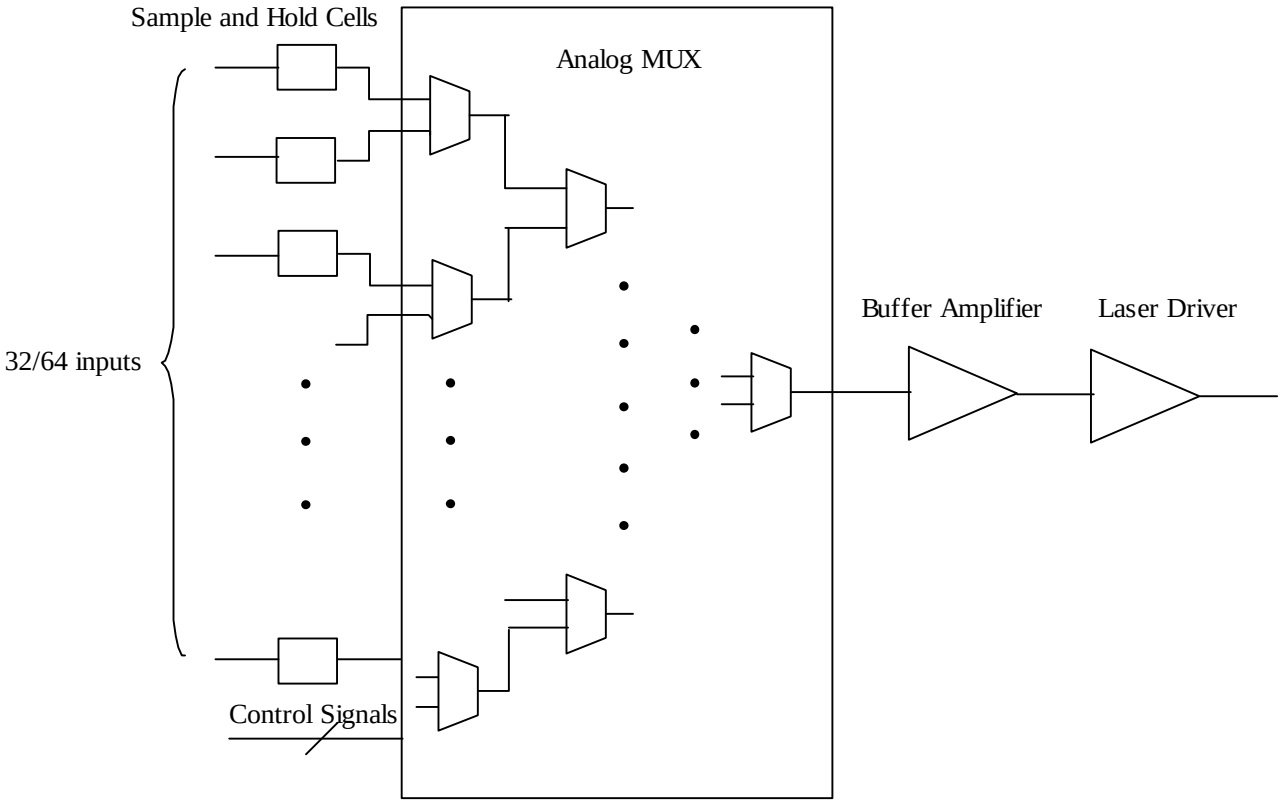

Figure 20: PIXRO1 Method 1 Configuration

5.3.2. PIXRO1 Method 2: High-speed Analog Multiplexer

The idea of Method 2 is that there is only a small area of the Pixel detector, which matches charged particle tracks identified by the rest of the Belle detector. In other words, at most something like approximately one tenth of the whole detector supplies the real useful information. The rest of the area just supplies the background information. In other words, only part of the data is real “interesting”. So in Method 2, only the

"relevant data" is further processed and sent to the back-end electronic block. Those interesting data are further skimmed into clusters to reduce the data volume.

The configuration of the second method is shown in Figure 21. After all the signals from the Pixel detector are sent into the Analog RAM (Random Access Memory), the addresses indicating the signals which are in the areas of interest come from the Back-End, and only the relevant data are finally broadcasted to the output of the RAM and to the readout FINESSE board.

This method significantly reduces the volume of data that needs to be processed. As a result, it reduces the event latency. Additionally, this method does not need an ADC on the front-end. The potential disadvantage is that it might eliminate some useful information since only part of the Pixel frame is recorded.

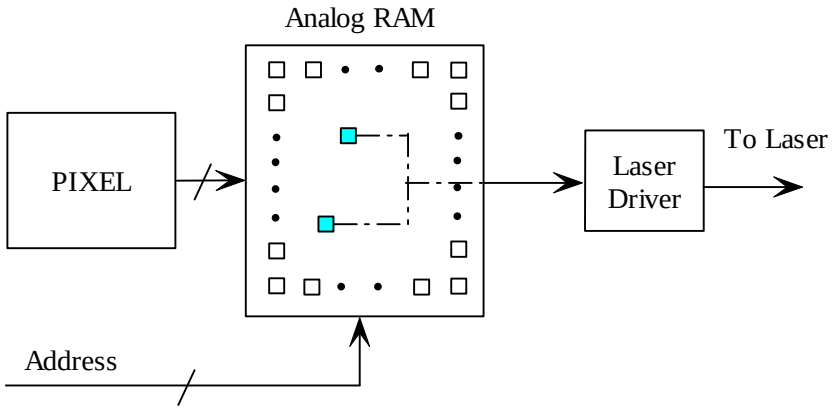

Figure 21: PIXRO1 Method 2 Configuration

5.3.3. PIXRO1 Method 3: Conversion and Compression Digital Transfer

There are two configurations are proposed for Method 3. Figure 22 illustrates the first configuration. The analog signals from up to 64 channels are pipelined into a memory, followed by an ADC module to convert them to digital signals, and then the multiplexer transforms them to series signal, finally the signals are send to the laser driver. The memory structure can be as same as the sample and hold cells used in Method 1, or it can be more complex depending on the pipeline scheme. Also depending on the pipeline scheme, the ADC module can be composed of a single ADC or several parallel ADCs. The bottleneck of this design is its dependency ADC sampling speed.

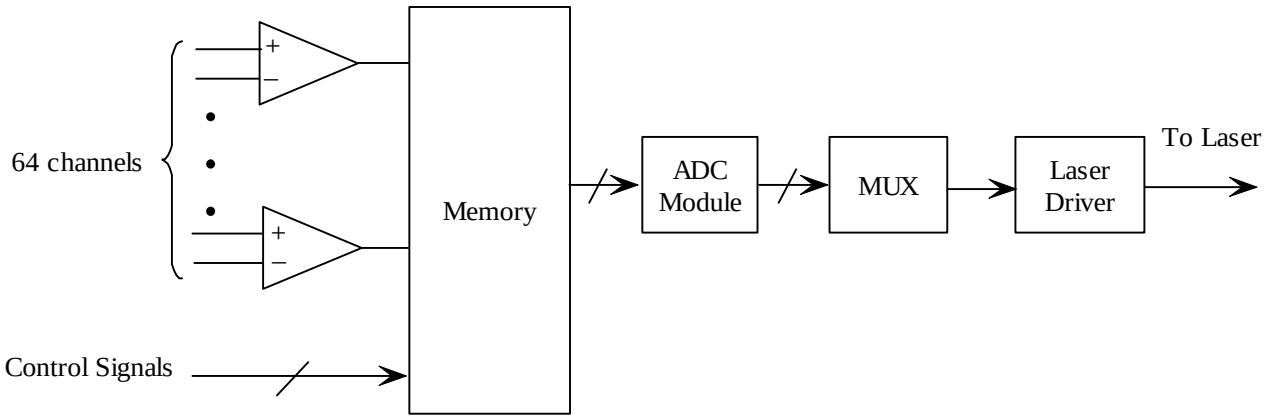

Figure 22: First Configuration of PIXRO1 Method3

The second configuration is illustrated in Figure 23. All the analog signals are digitized after passing through an array of ADCs. The multiplexor pipelines the signals and their signals into a RAM array. Then their values are scanned and compared with their threshold values, which are stored in another RAM. If the difference exceeds threshold, cluster data only is sent. The analog values and address of those hits part of the cluster is set to the laser driver. In this way, the data needs to be sent to the back-end electronics can be greatly reduced.

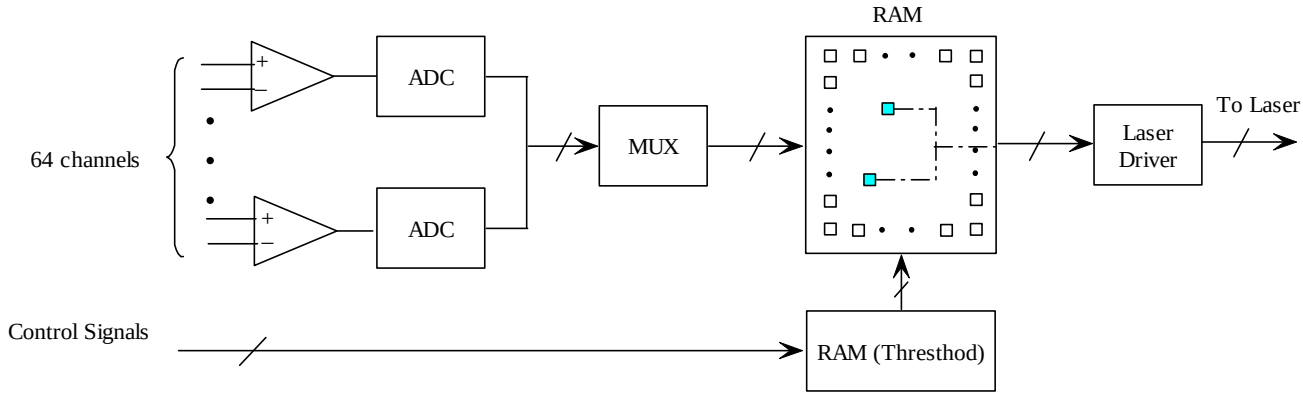

Figure 23: Second Configuration of PIXOR1 Method 3

PIXRO1 Method 4: Digital Pulse Width Modulation

Method 4 utilizes a scheme of voltage to time modulation (Figure 23). As shown in Figure 24, the input signal of V-t Modulator has different amplitude, a and b. During the sample time, which is the time of high voltage of the reference clock of modulator, the duty cycle of the output will be adjusted corresponding to the input amplitude, as a' and b'.

The advantage of this method is that the circuit for modulation structure is simple, by employing a voltage comparator. Moreover, the output is a digital signal which avoids absolute DC level problems. However, this method is limited by the accuracy of the time base sample.

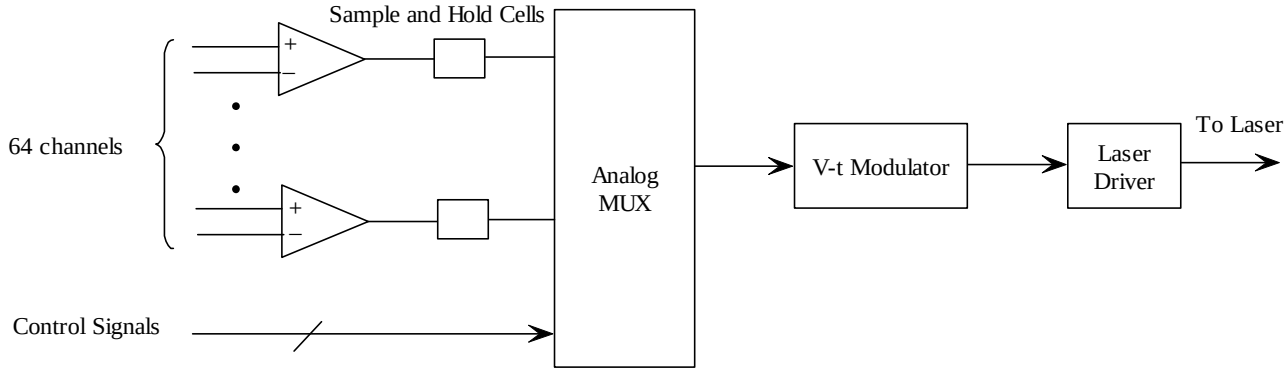

Figure 6: PIXOR1 Method4 Configuration

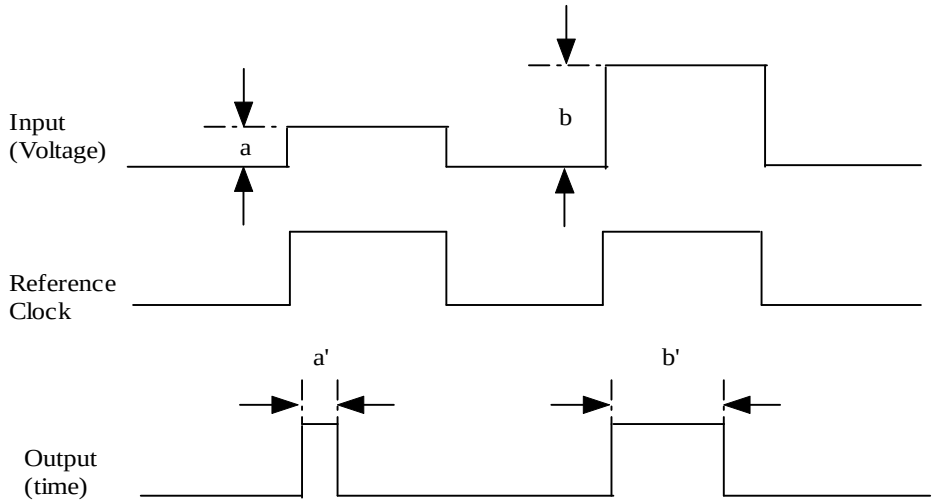

Figure 24: Voltage to Time Modulation

6. Plans and Schedule

Evaluation of the CAP2 pixel pipelined operation will be performed during at the T943 beam test during December 2004 at Fermilab. Further evaluation of the CAP3 pixel prototype will be performed at KEK during the summer of 2005. Based upon positive results of these evaluations, a formal proposal for the fabrication of a pixel vertex detector will be made in the form of a Technical Design Report.

7.References

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2. There are many concurrent efforts going on worldwide and this listing is meant to be indicative only:
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   A pointer to the LBNL/STAR effort: H.S. Matis *et al*., IEEE Trans. Nucl. Sci. **50**: 1020-1025, 2003.
3. G.Varner, "XTEST2 Design Report: Design Reference and Functional Description of the First Belle Pixel Readout IC", Belle Note #278, Dec. 1999.
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