# Development of Monolithic Active Pixel Sensors for a Belle Vertex Detector Upgrade and ILC Inner Vertexing

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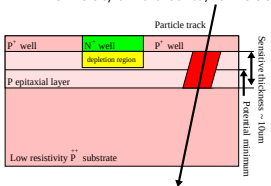


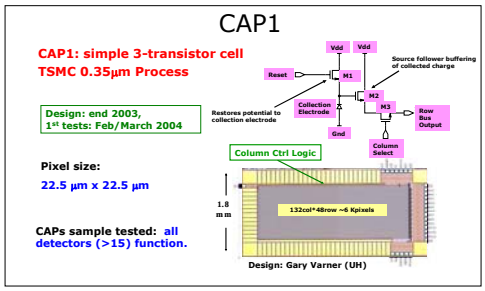

**Key Features:**

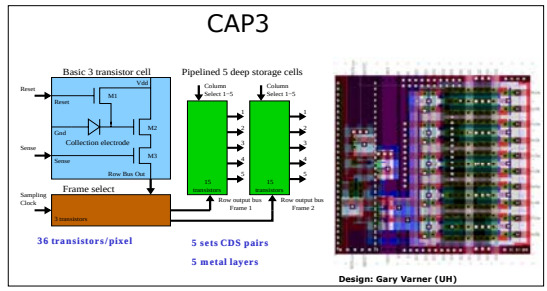
- q collection via thermal diffusion (no HV)
- "System on Chip" possible
- NO bump bonding (not a hybrid pixel detector)
- Could be thinned.
- Standard CMOS: good process control, low cost…

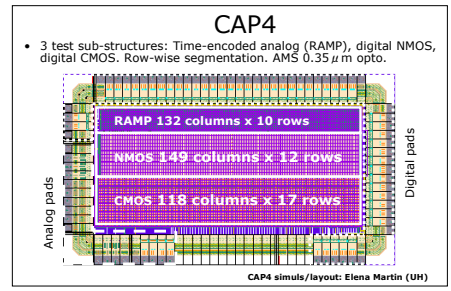
**Principle of operation:** When a charged particle passes through a **M**onolithic **A**ctive **P**ixel **S**ensor (**MAPS**), it creates electron-hole pairs in the epitaxial layer. The electrons that are created are then collected in the N wells by thermal diffusion (no high voltage is needed) whereas they bounce off the P++ / P interfaces because of a potential barrier.

**Prototypes:** The **C**ontinuous **A**cquisition **P**ixel (**CAP**) prototypes consist of an array of pixel cells. The base structure of the pixel cell is the standard 3-transistor cell used to build up MAPS: reset, sense, and select transistors. A circuit infrastructure is built around the array to read out as fast as possible. Correlated double sampling (CDS) read-out scheme is used. CAP1-3 were made by Taiwan Semiconductor Manufacturing Company (TSMC).

- **CAP1:** An array of 132x48 3-transistor pixels with 0.35μm feature size. The pixel size, 22.5 x 22.5 μm², was chosen to minimize the number of readout pixels while still obtaining excellent single point resolution. It was succesfuly operated in a $\pi$ beam test at KEK – resolutions measured with a 3 plane telescope.
- **CAP2:** Same pixel size, no. of pixel and feature size as CAP1. Has an 8-deep pipeline for data storage inside each pixel cell besides the basic 3 transistors. Should handle a sampling speed of 100kHz and external triggering. 10μs frame acquisition speed achieved, too noisy for a successful beam test.
- **CAP3:** The size of the array was increased from 132x48 to 928x128 pixels, 0.25μm feature size. Each pixel contains a 5-deep double pipeline for differential readout. A sensor of this size (3 x 21mm²) could be used as a building block for an actual detector. Successful test with a laser probe station.
- **CAP4:** being fabricated in the AMS 0.35μm "opto" (thick epitaxial) process, available for test in late fall 2006. It will explore a faster version of CAP3 readout as well as two different "digital" techniques.

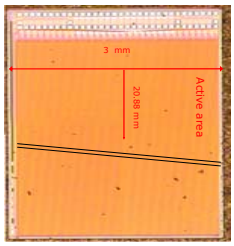


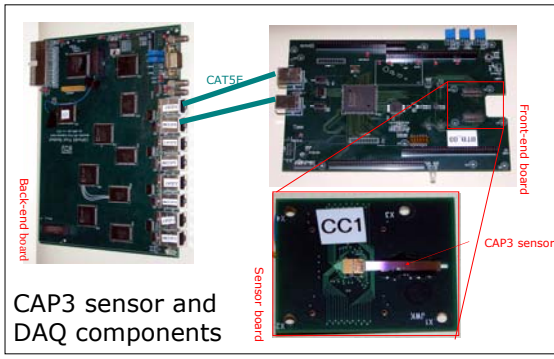




**Experience with CAP3:** A two-card scheme is used for the CAP data taking. The CAP sensor module is plugged into a Front-End Board with 10-bit ADC and analog support electronics. This Front-End Board communicates via CAT5E cables with a Back-End Board located inside a Compact PCI (cPCI) crate. Data is broadcast over a high-speed LVDS serial link operating at approximately 400Mb/s to Back-End and waits for RAMs to be read out by a CPU-card through the cPCI interface. We were able to see clear signal of the λ=980nm IR laser beam illuminating CAP3 from the back side through 250μm of silicon. We discovered that 16 groups of rows connected to different multiplexers behave differently in terms of noise and there is a systematic shift in transfer curve response across the length of the chip. With a row-wise scan we also discovered there may be some crosstalk or scrambling between these 16 regions. All these issues to be investigated further and gain correction established.

## CAP3 sensor in detail



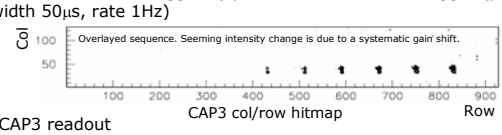

928 x 128 pixels = 118,784
~4.3M transistors !




CAP3 sensor and DAQ components

## CAP3 IR laser testing

- Laser spot from a λ=980μm IR laser moving on the backplane surface of CAP3, spot size <100μm. Data taken with 1) continious beam and random trigger 2) pulsed beam with and trigger (pulse width 50μs, rate 1Hz)

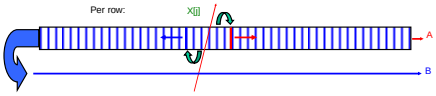



- CAP3 readout
  - only partial pipeline read so far (full pipeline readout still to be checked)
  - recording differential value of the CDS, plan to measure also absolute frame value with an additional readout board to correct for the gain shift
- Laser test station ready for CAP4 testing

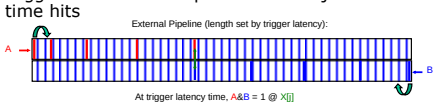
**Purpose of CAP4:** attempt to **fix the problems encountered in CAP3** *(limited dynamic range, poor choice of the reset transistor control, long settling time on highly capacitive (long) bus lines (~1μs), large drive strength needed for fast, unbuffered signals)* in a **new, faster, time-encoded analog CAP4 scheme** (*redesigned reset transistor circuit, Wilkinson type readout with voltage ramp (analog → time), improvement in the drive of a line*) and **test 2 new digital designs** with radically different architecture (smaller pixels, binary continuous readout, no trigger rate limitation)

## CAP bin

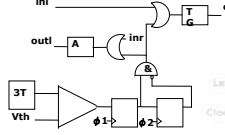
- Binary readout; if pixel size reduces to 11.25μm, intrinsic resolution ~3.25μm
- 100ns sample steps – values shifted out left/right




- Use temporal coincidence and match with trigger to reconstruct position and reject out of time hits

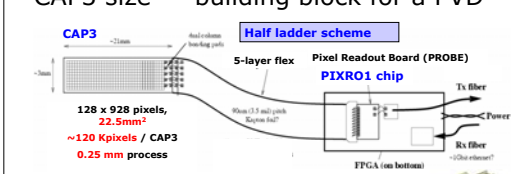


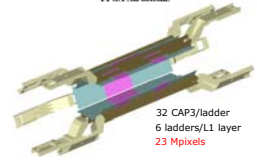

## CAP4 binary architecture




- Output bits can be multiplexed onto LVDS lines
- Natural zero suppression with trigger matching
  - No "long lines"
  - No complex buffer matching
- Coincidence pipeline implemented in standard FPGA

## "CAP3 size" – building block for a PVD




**Towards a full PVD:** CAP5 prototype may again be of the "building block size" for construction of a Super B factory PVD. Its design will depend on the CAP4 test results (laser scan, radioactive source testing, beam-test) and the development of the SOI prototypes. Readout may move to FINESSE/COPPER system being developed for Super Belle. Critical requirements (readout speed, radiation hardness, full sized detector) were matched "per partes" in different CAP prototypes, but not yet all of them in one. CAP5 may be it.