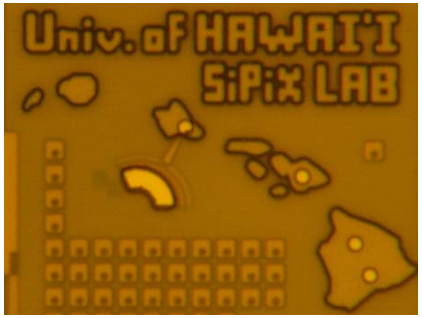
Development of a Monolithic Active Pixel Detector for a Super-B factory

Marlon Barbero, University of Hawaii

On behalf of the Belle Pixel Group
KEK, Krakow INP, Univ. of Hawaii, Tsukuba Univ.

DPF Riverside – 27-31 August 2004

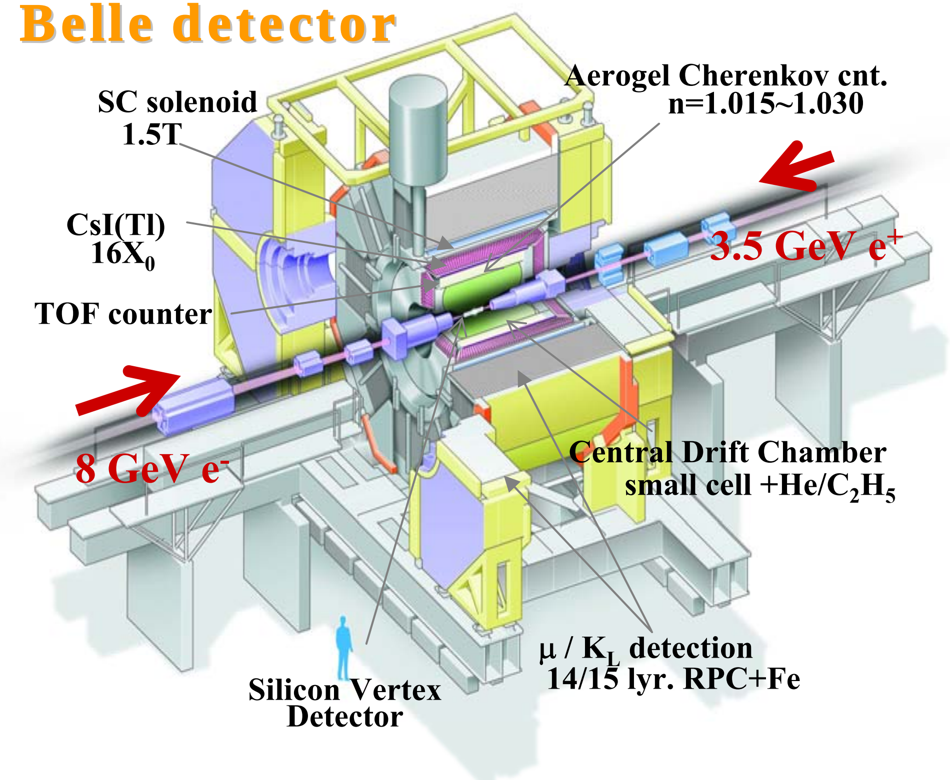


Outline

- → **KEKB and BELLE detector.**
- → **BELLE Silicon Vertex Detector / Super-BELLE perspective.**
- → **Monolithic Active Pixel Sensor (MAPS) for BELLE upgrade.**
- → **Principle of MAPS.**
- → **Results of beam test on prototype MAPS, summer 2004.**
- → **Critical R&D items.**
- → **Plans for the near future.**
- → **Highlights and conclusion.**

BELLE detector at KEKB

Belle detector



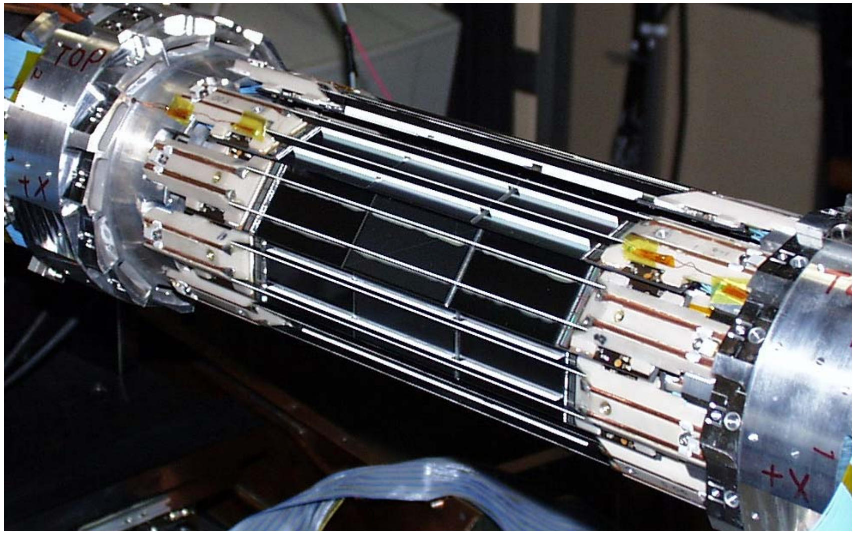
KEKB / Belle started operation in 1999

8 GeV e^- x 3.5 GeV e^+

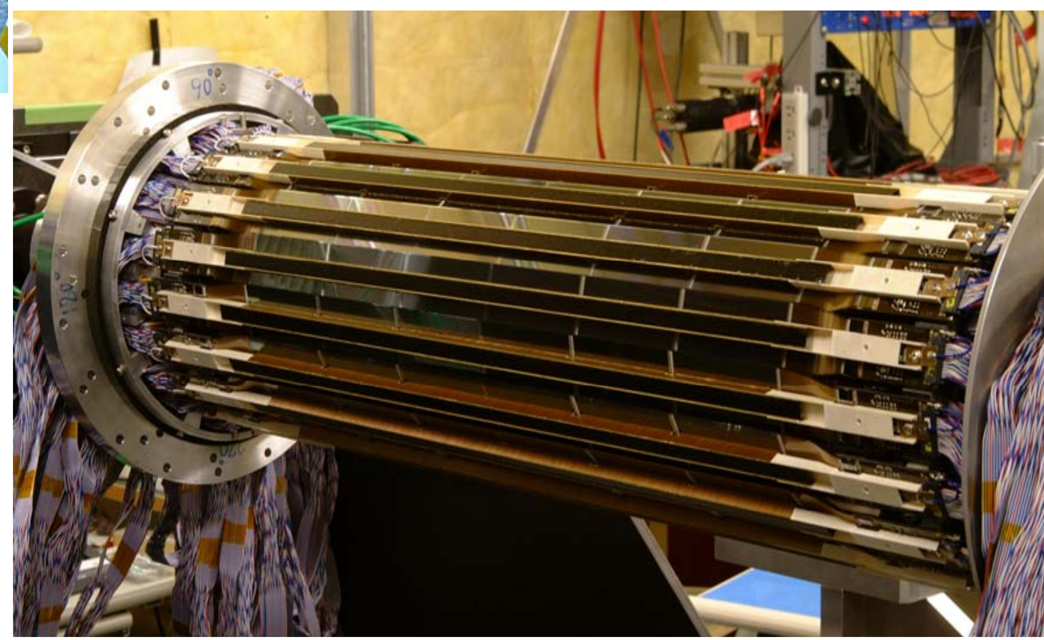
L_{peak} = 1.39×10^{34} cm^{-2} sec^{-1}
(highest peak luminosity)

Integrated Luminosity
250 fb^{-1} on-peak so far...
(~274 M. $B\bar{B}$)

BELLE SVD1 → SVD2



1st generation Silicon Vertex Detector (SVD1) → 2nd generation SVD (summer 2003)



Beam pipe radius: 20mm → 15mm

3 layers → 4 layers

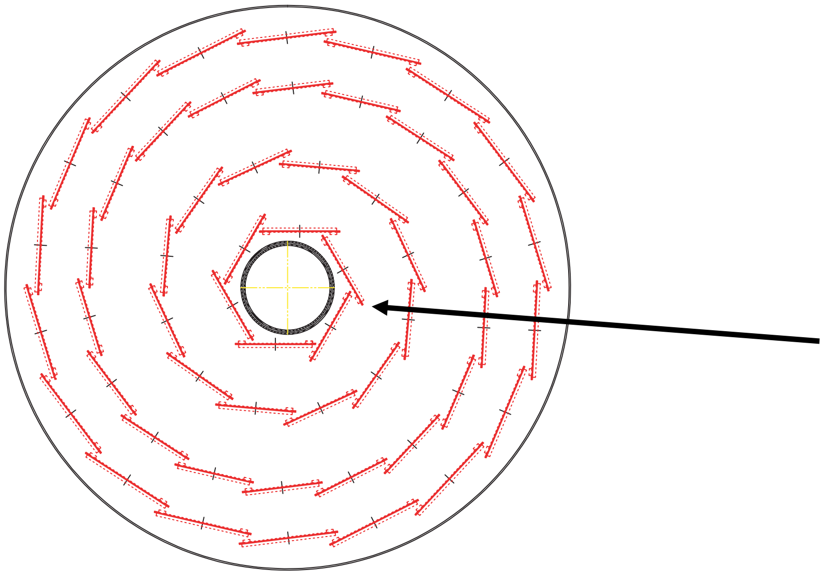
~82K channels → ~110K channels

23° - 139° → 17° - 150° coverage

R=30/45/60 → R=20/43/70/88 (mm)

$\sigma_{r\phi}$ 12μm/ σ_z 20μm

SVD with S-Belle perspective



Present : Belle SVD

~10% occupancy

200 Krad.yr^{-1} cumulated

Upgrade: Super-Belle $L \sim 1.10^{34} \rightarrow L \sim 5.10^{35}$ $cm^{-2}.s^{-1}$

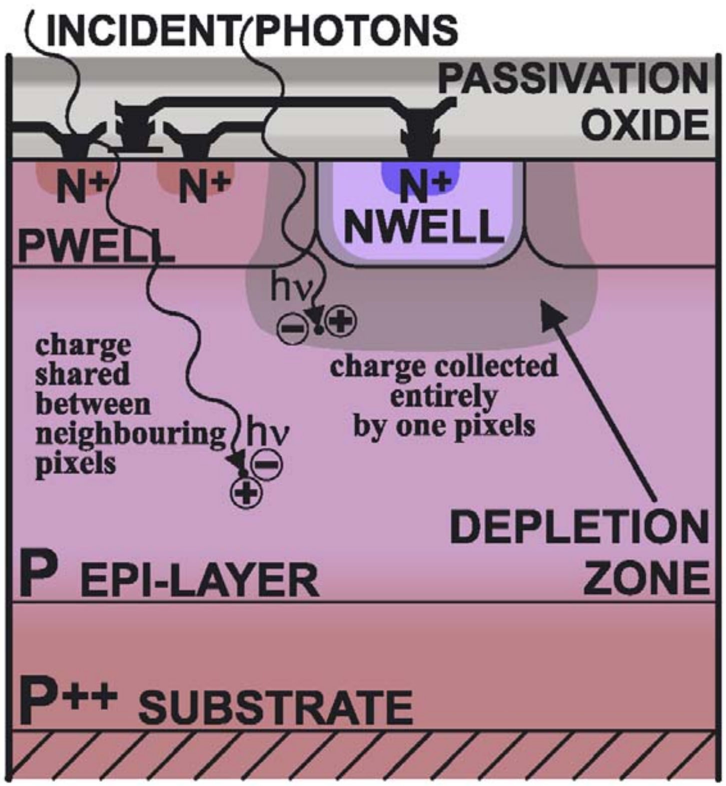
Background increase typ. x50 ! → Occupancy / dose:

Conventional solutions (Si strips) do not work.

Better impact parameter resolution?

MAPS Technology: Standard CMOS

"From digital camera to particle tracking device"



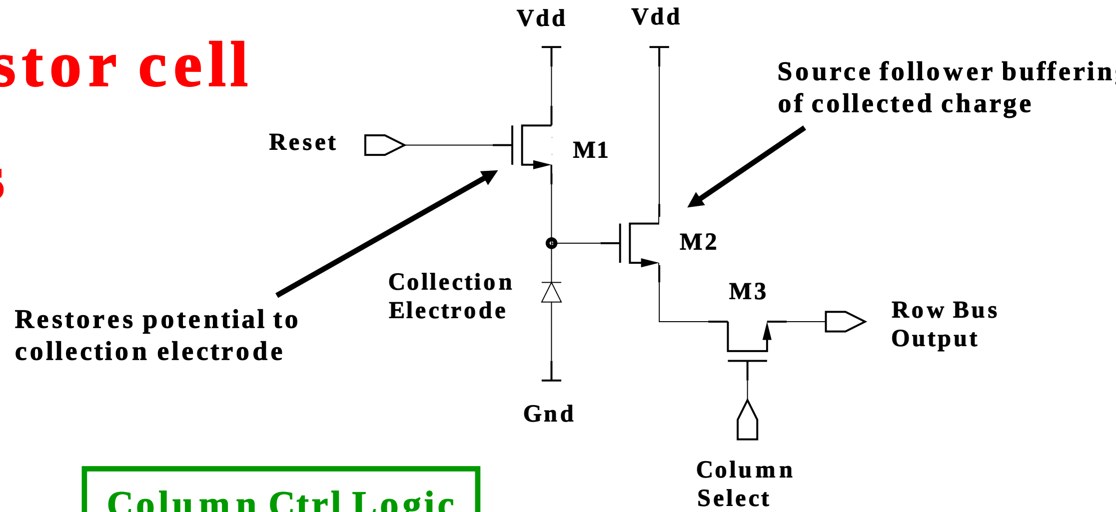
Key Features:

- **q collection via thermal diffusion (no HV)**
- **"System on Chip" possible**
- **NO bump bonding (not a hybrid pixel detector)**
- **Could be thinned.**
- **Standard CMOS: good process control, low cost...**

Cont. Acq. Pixels (CAP) 1 Prototype

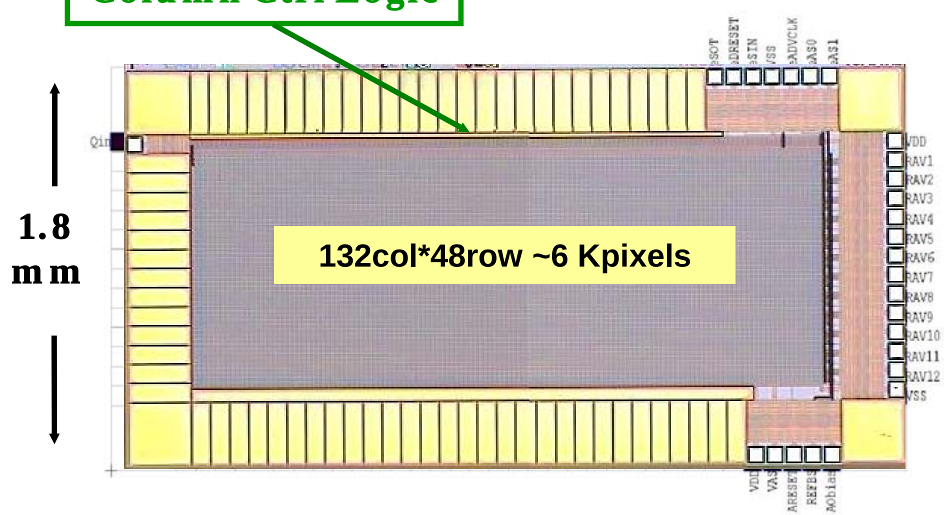
CAP1: simple 3-transistor cell

TSMC 0.35μm Process



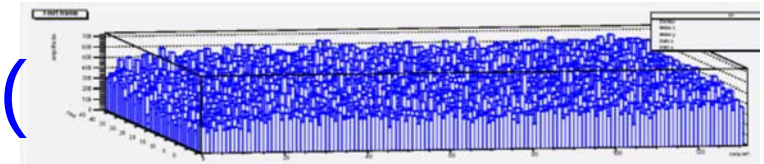
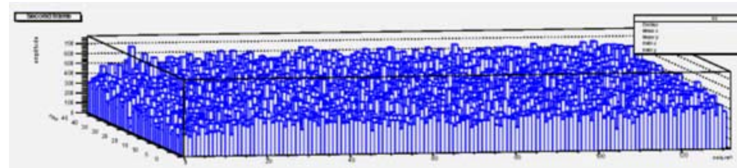
Pixel size:

22.5 μm x 22.5 μm

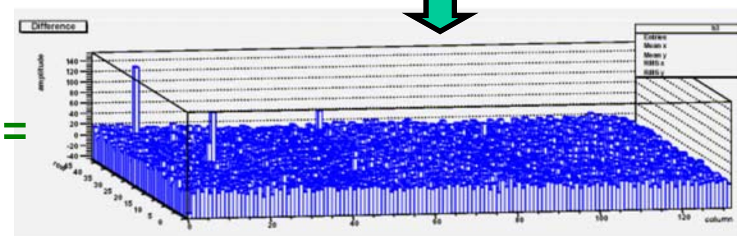


CAPs sample tested: all detectors (>15) function.

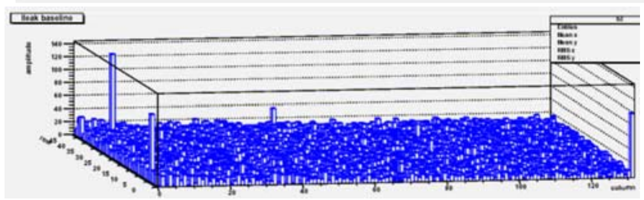
Correlated Double Sampling (CDS)

( - )

Frame 1 - Frame 2 =



- Leakage current Correction

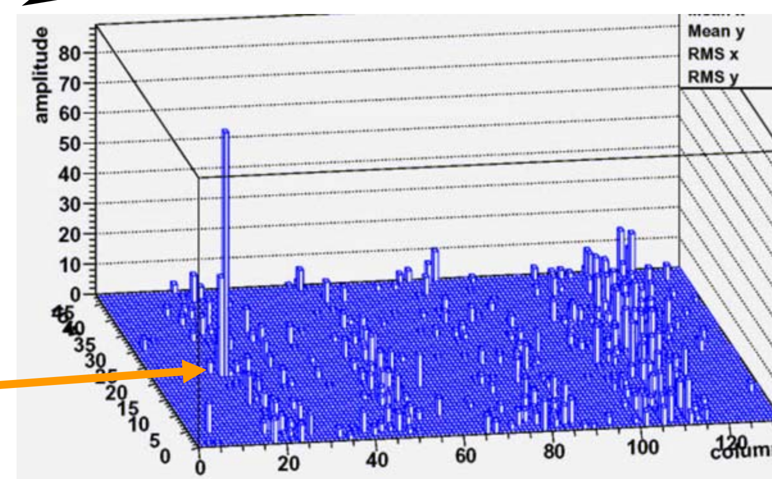


8ms integration

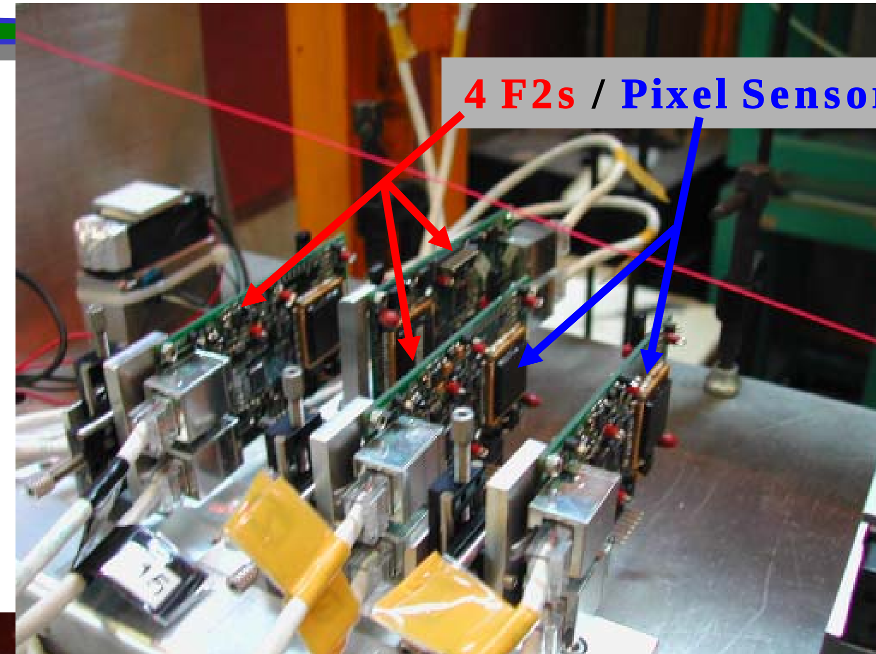
Can readout/process @ 20Hz ~ 16% live time (CAP1!) Self-Triggering mode

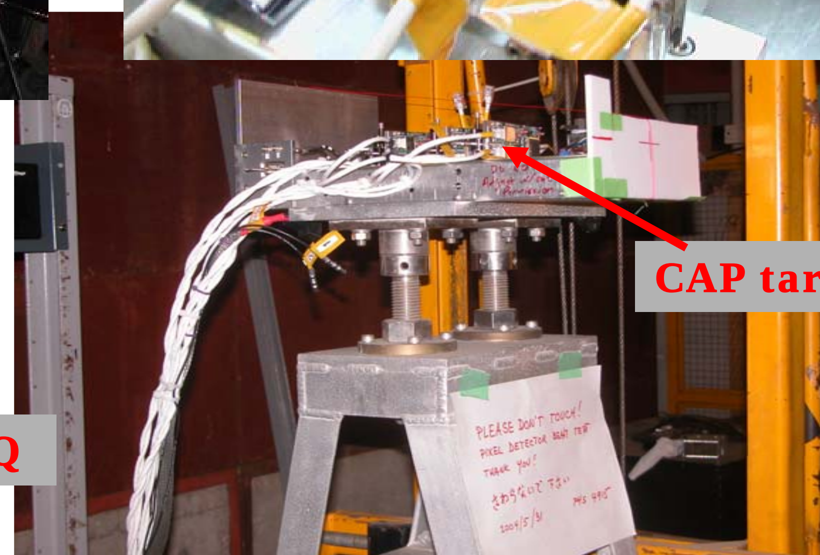
~fA leakage current (typ)
~18fA for hottest pixel shown

Hit candidate!

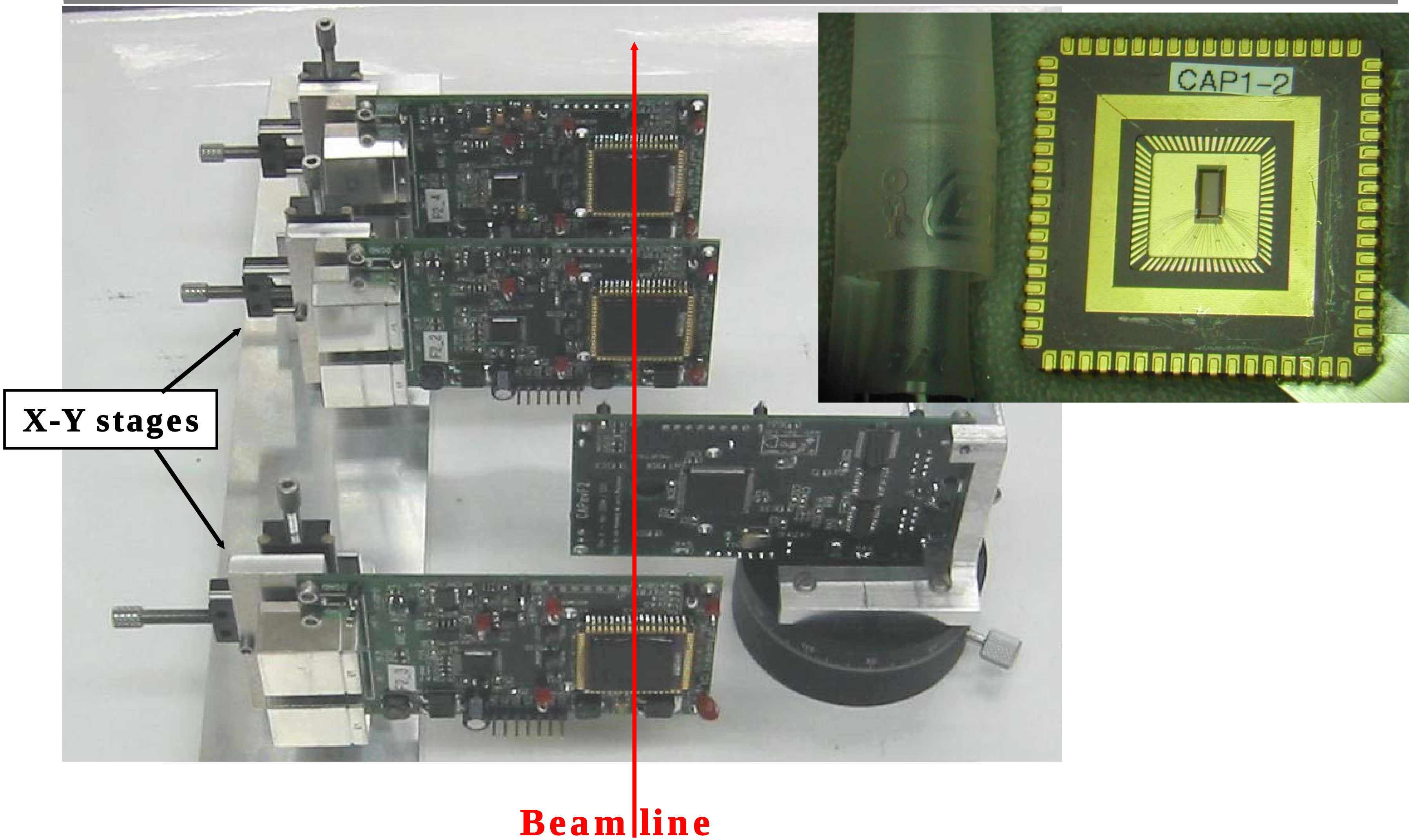


Jun.04 KEK Test Beam with pions



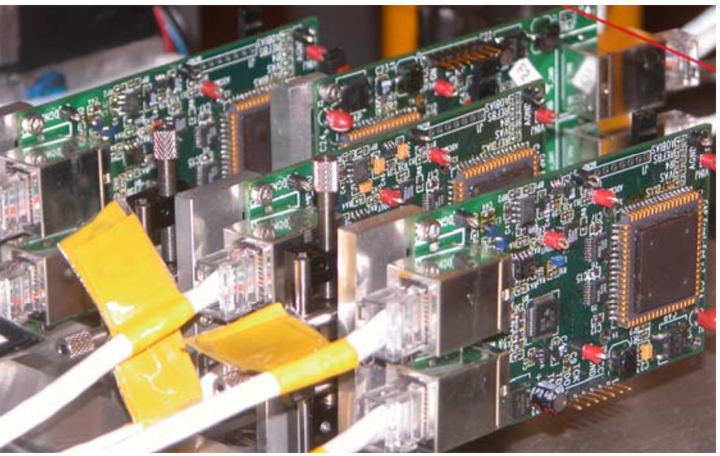


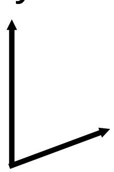
Beam test bench



Initial “by eye”

~1mm x 3mm “rice grain”

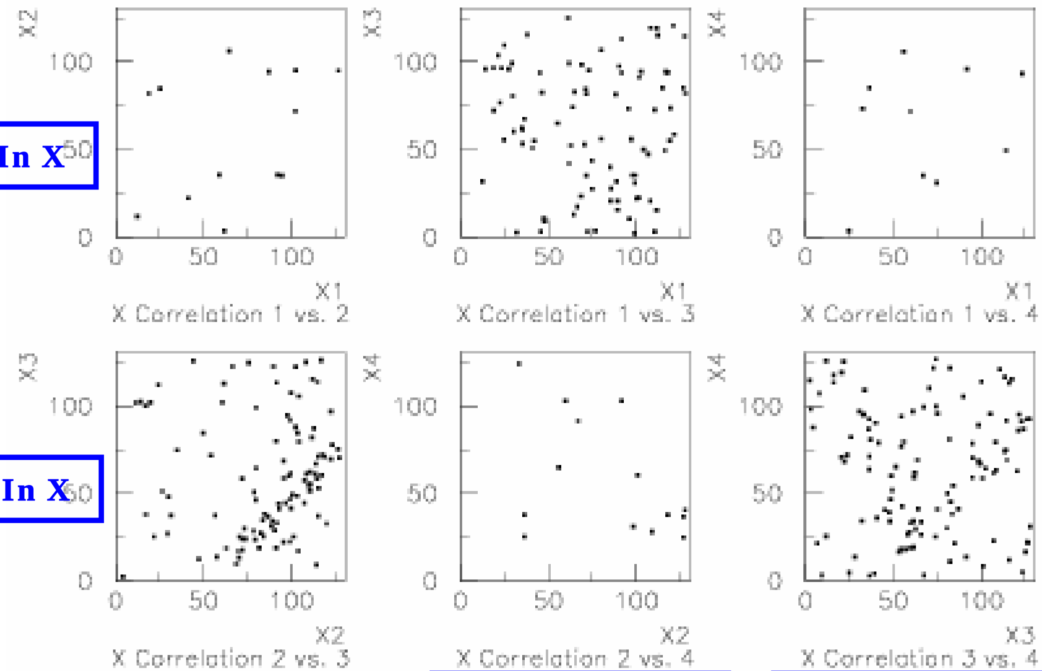




Layer-by-layer correlations

Det.3 vs. Det.1 **Det.3 vs. Det.2** **Det.3 vs. Det.4**

In X



In X

Det.3 vs. Det.2 **Det.4 vs. Det.2** **Det.4 vs. Det.3**

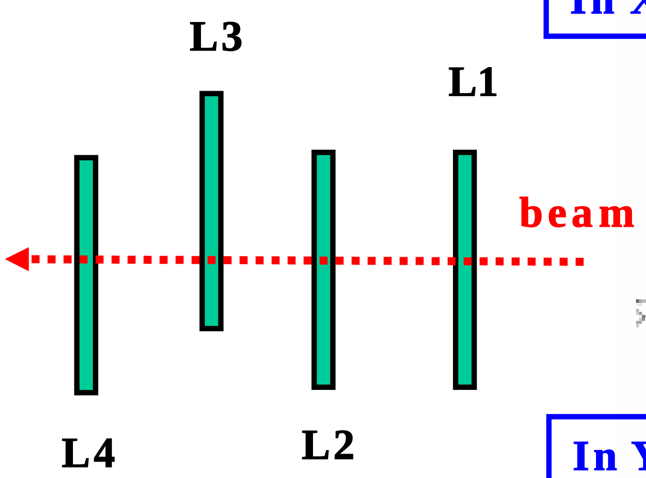
And after 4 iterations…

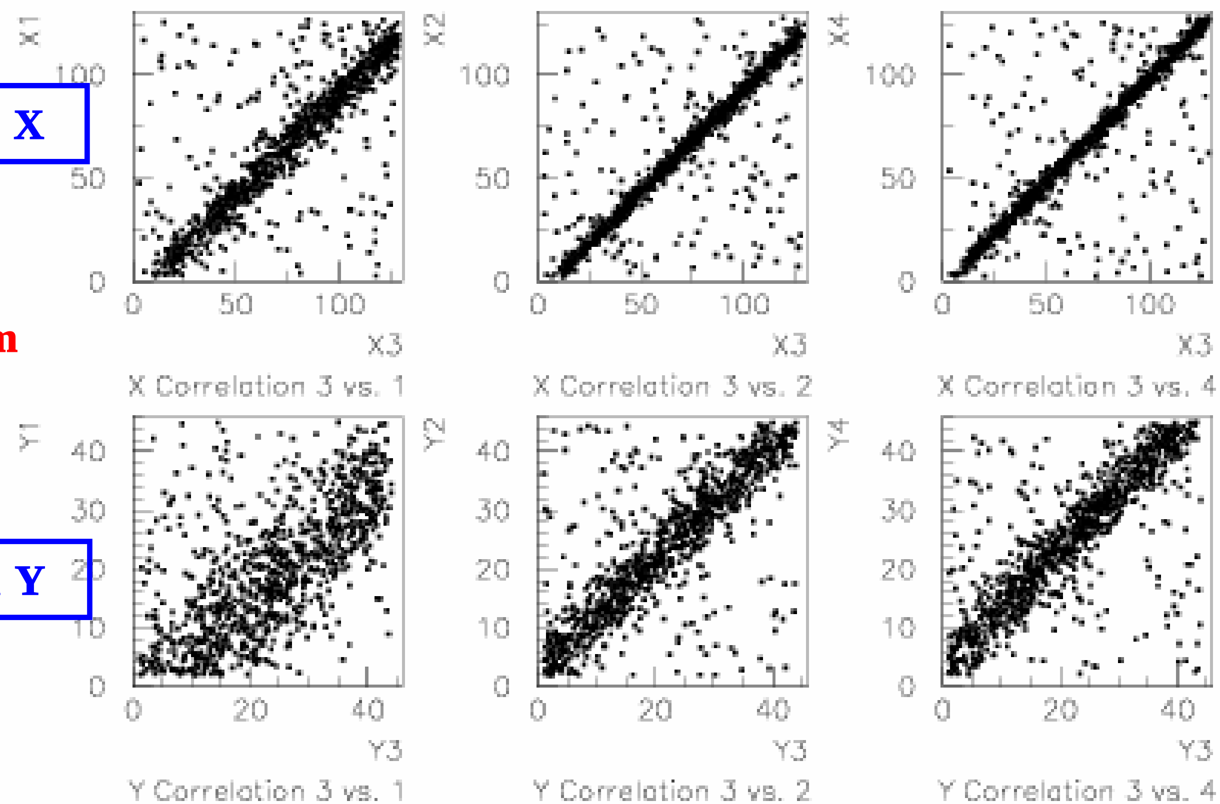
Improved Alignment

Det.3 vs. Det.1 | Det.3 vs. Det.2 | Det.3 vs. Det.4

In X

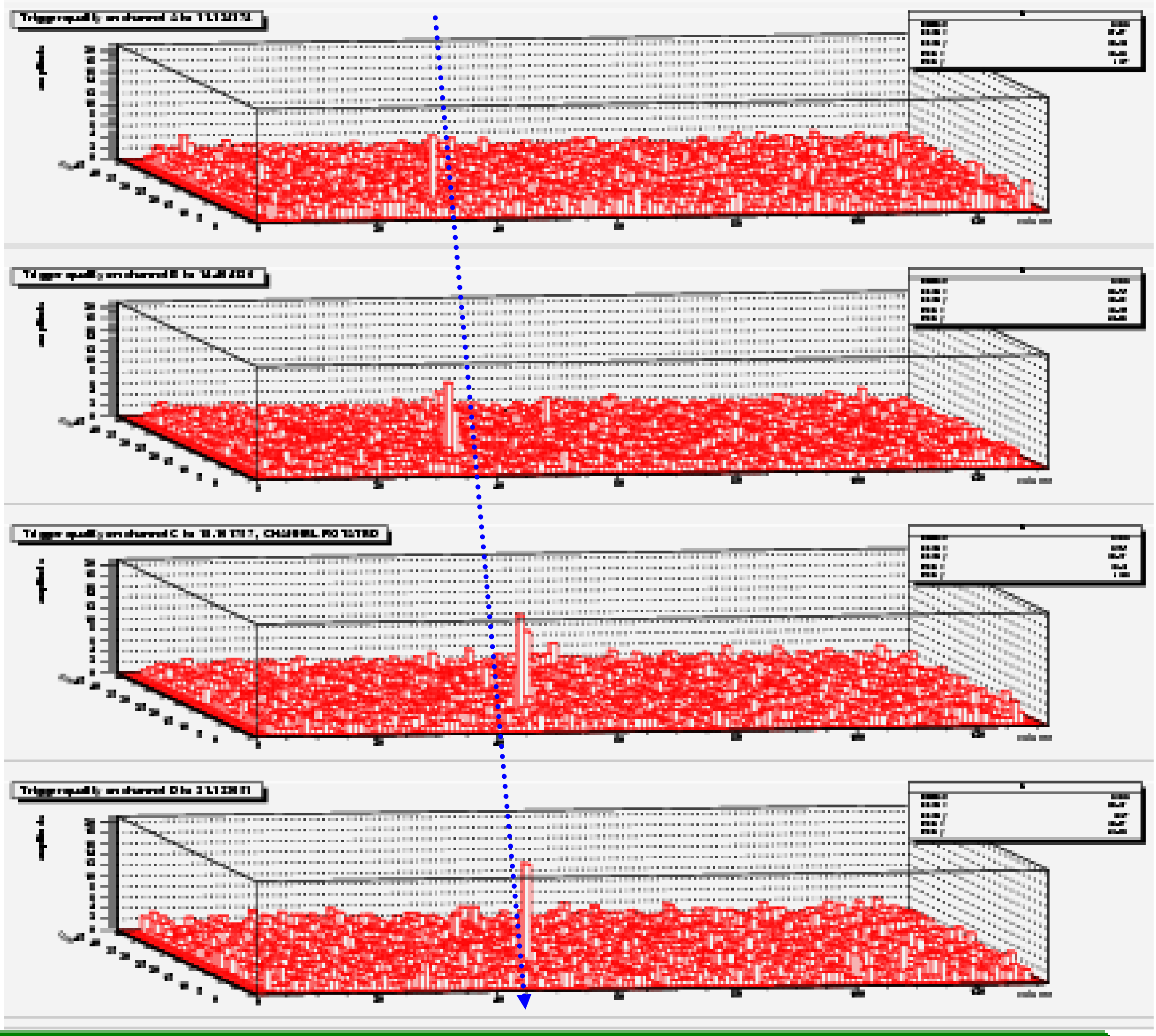
In Y



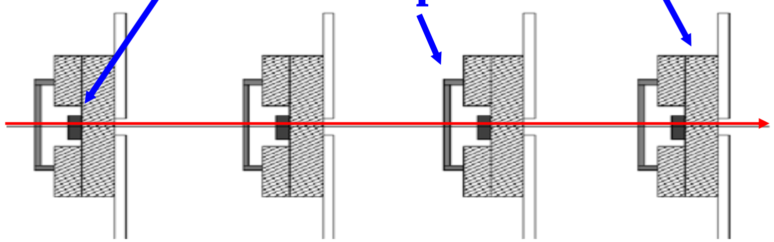


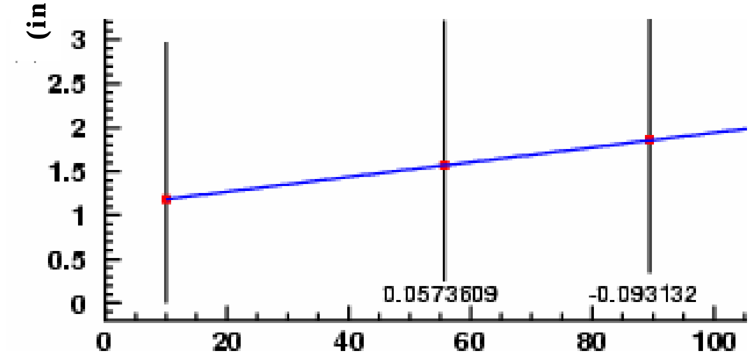
"online" plot

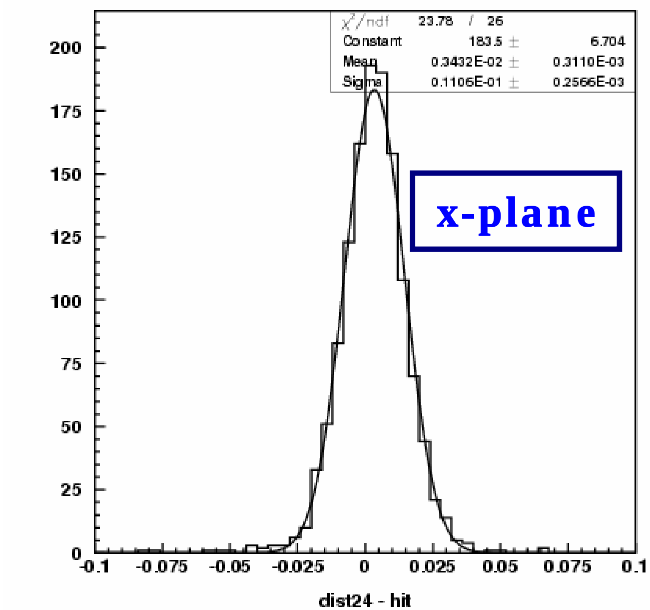
Hits! alignment proof



Hit resolution measurement





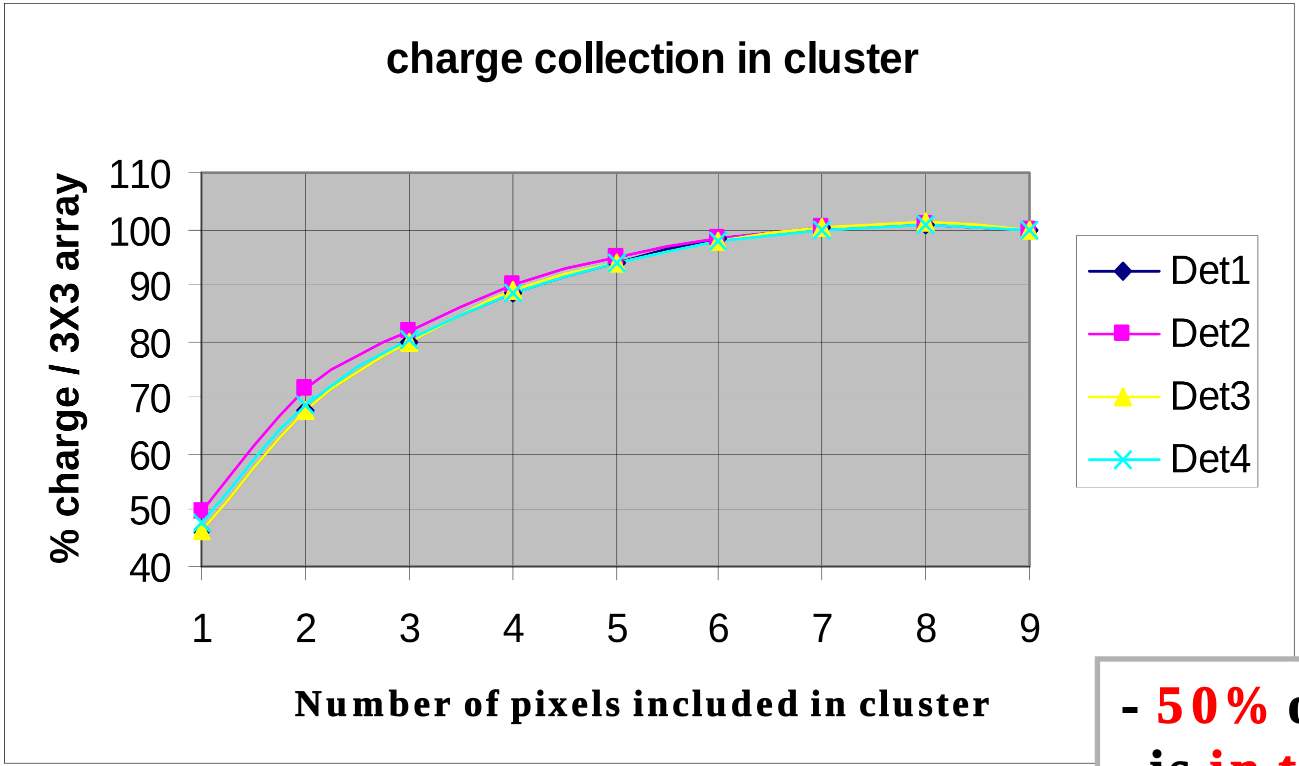


Current Residuals, @ 4GeV:

- **11μm in x plane**
- **14μm in y plane**

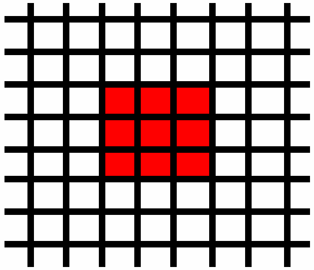
Charge Spread in CAPS

... still June 2004 beam test data...



(MPV of landau fit)

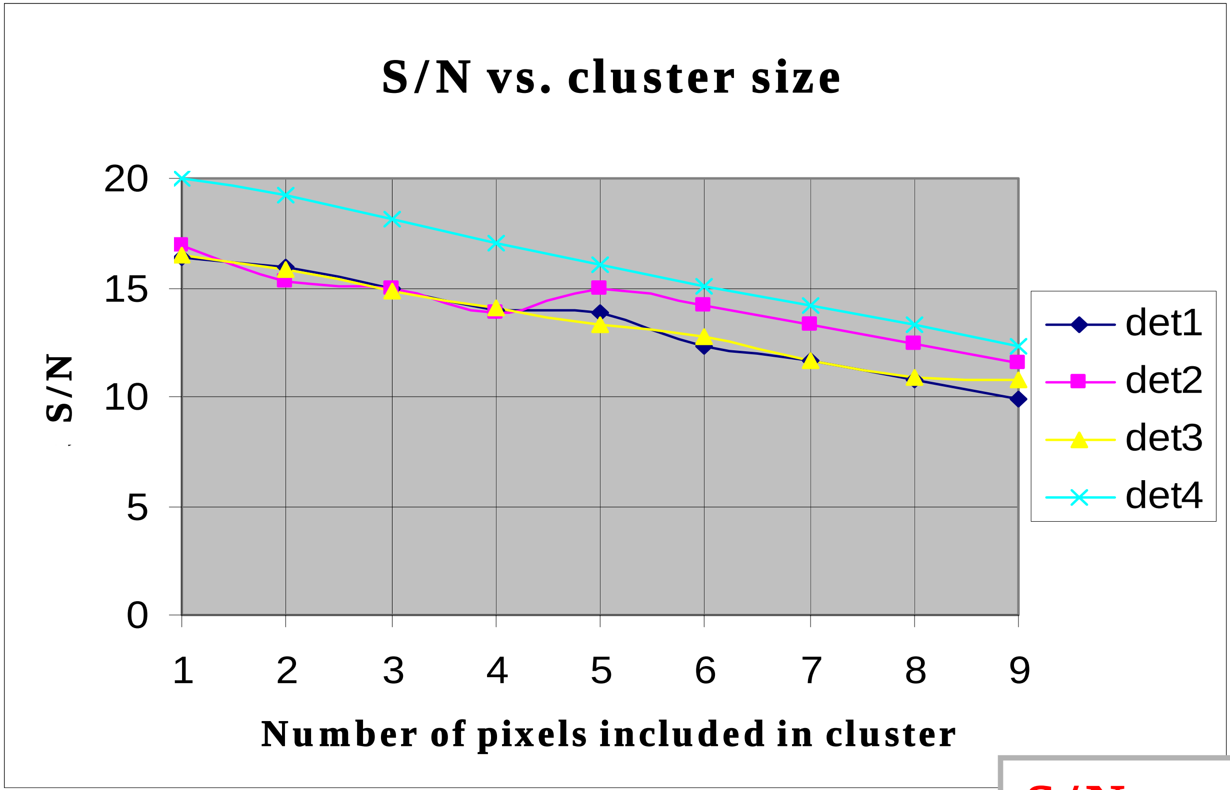
Hyp: charge entirely collected in 3X3 pixel array.

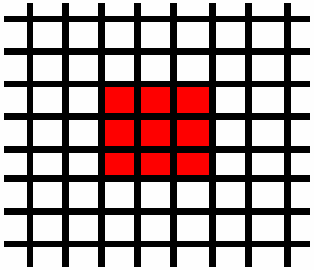


- 50% of the charge is in the peak pixel.
- 90% in the 4 largest.

S/N vs. Cluster Size

... still June 2004 beam test data...





S/N peak signal between 16 and 20.

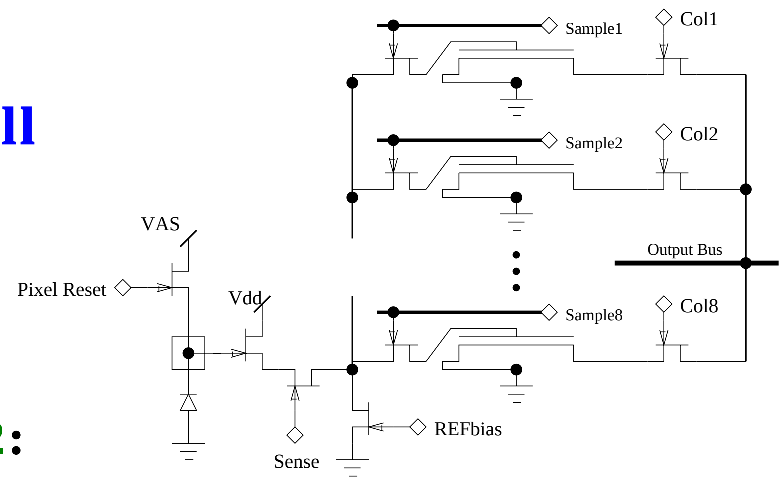
CAP1 / 8ms integration time

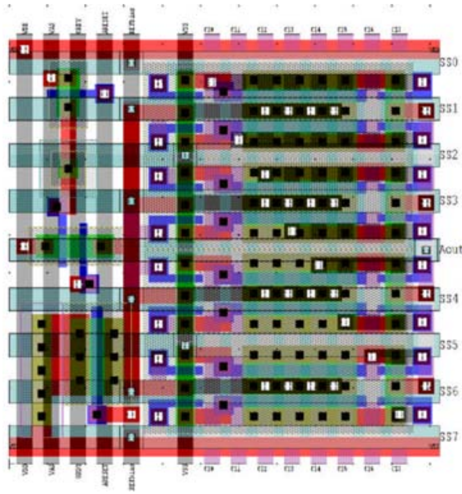
Four Critical R&D Items

1. **Readout Speed**
   1. **Super-B**: CAP2, syst. archi., next main R&D topic
   2. **Elsewhere**: STAR phase 1, LC, RAL efforts
2. **Radiation Hardness**
   1. **Super-B**: low E e^-/γ CAP -- results shown next
   2. **Elsewhere**: TESLA, STAR 10^{12} n_{eq}, >100kRad ionizing
3. **Thin Detector – LBNL**
4. **Full-sized detector – LEPSI**

1. Increased readout speed: CAP2

CAP2: 8x mini-pipeline in each cell



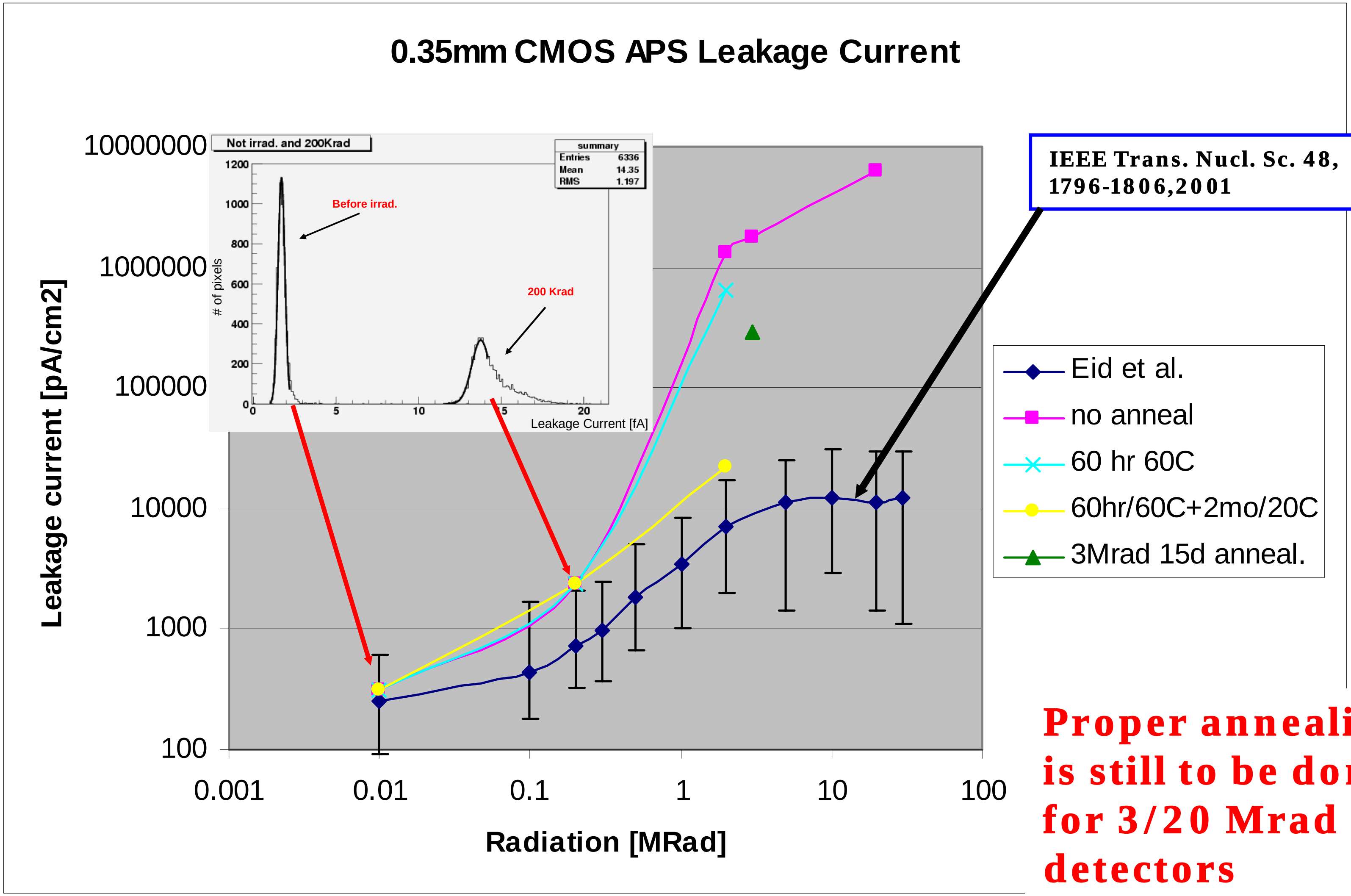


15μs operation of CAP2:

Current status:

- **Noise higher than what is observed with CAP1/F2/B2 (~30/~35e- vs. 16e-). Related to digital activity? → Shield?**
- **Leakage current under control.**
- **Mini-pipeline output level dispersion rather large.**
  Not a dramatic problem, but can improved (by design).
  → Modification in pipeline design?
- **Still more work to be done on CAP2 testing.**

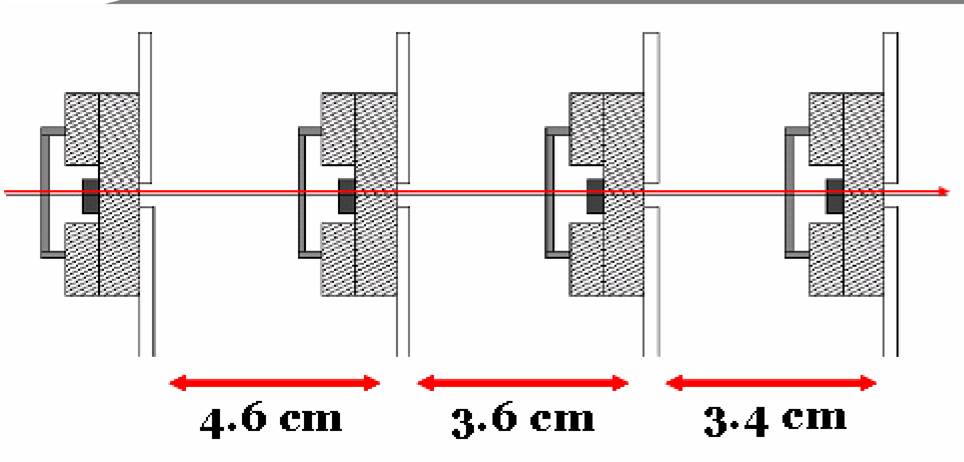
2. Irrad: leakage currents

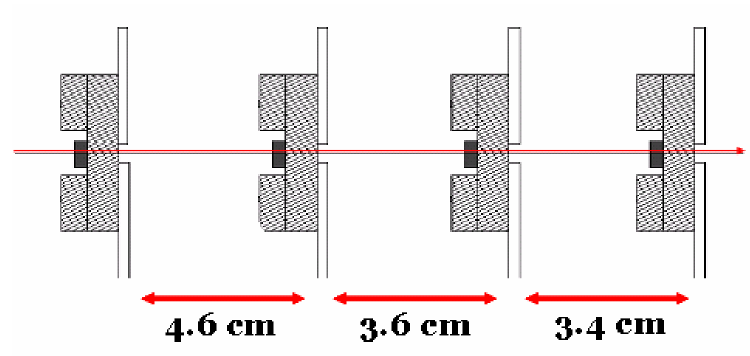


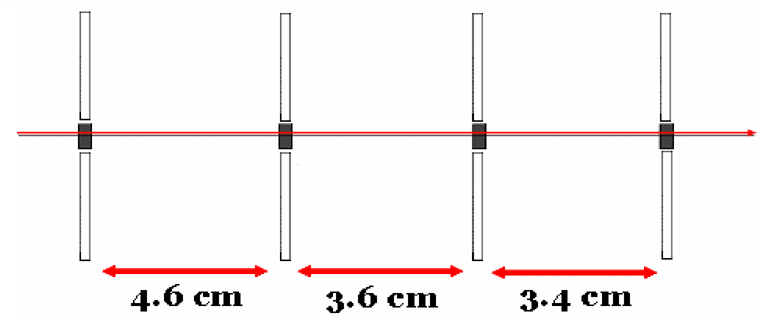
IEEE Trans. Nucl. Sc. 48, 1796-1806,2001

Proper annealing is still to be done for 3/20 Mrad detectors

Improving the UL on resolution?





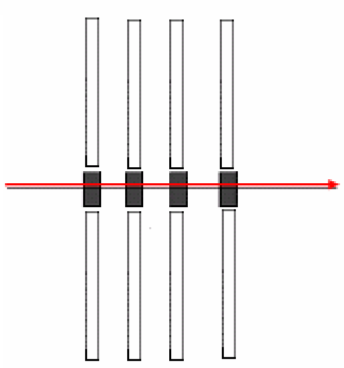


1- no cover

2- no die package behind sensor

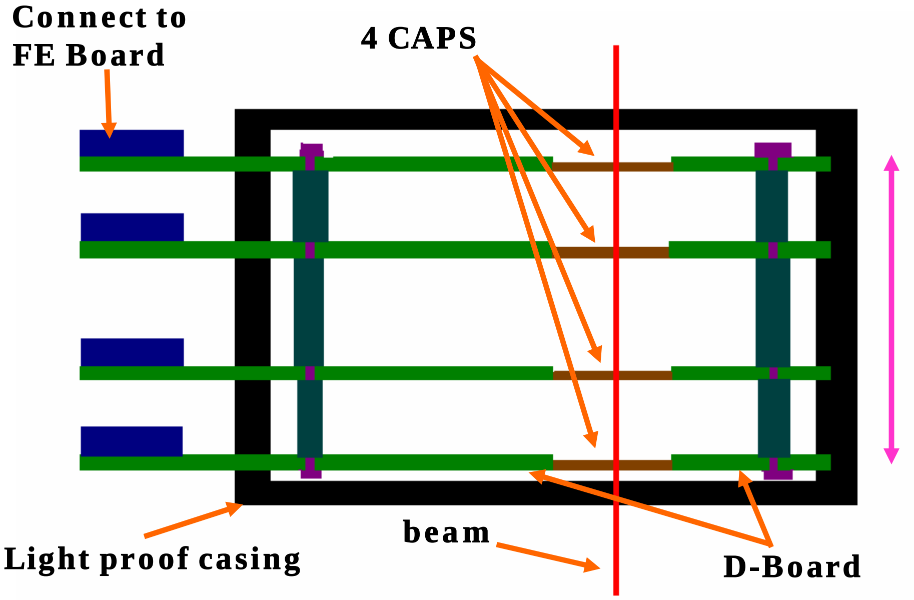
3- attach die to board

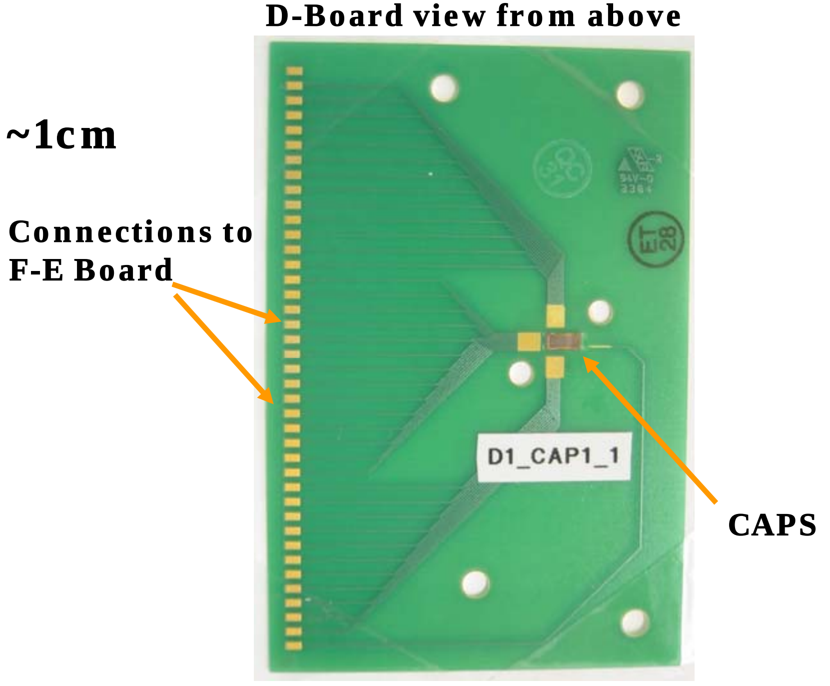
4- move the boards closer



Improving the UL on hit resolution

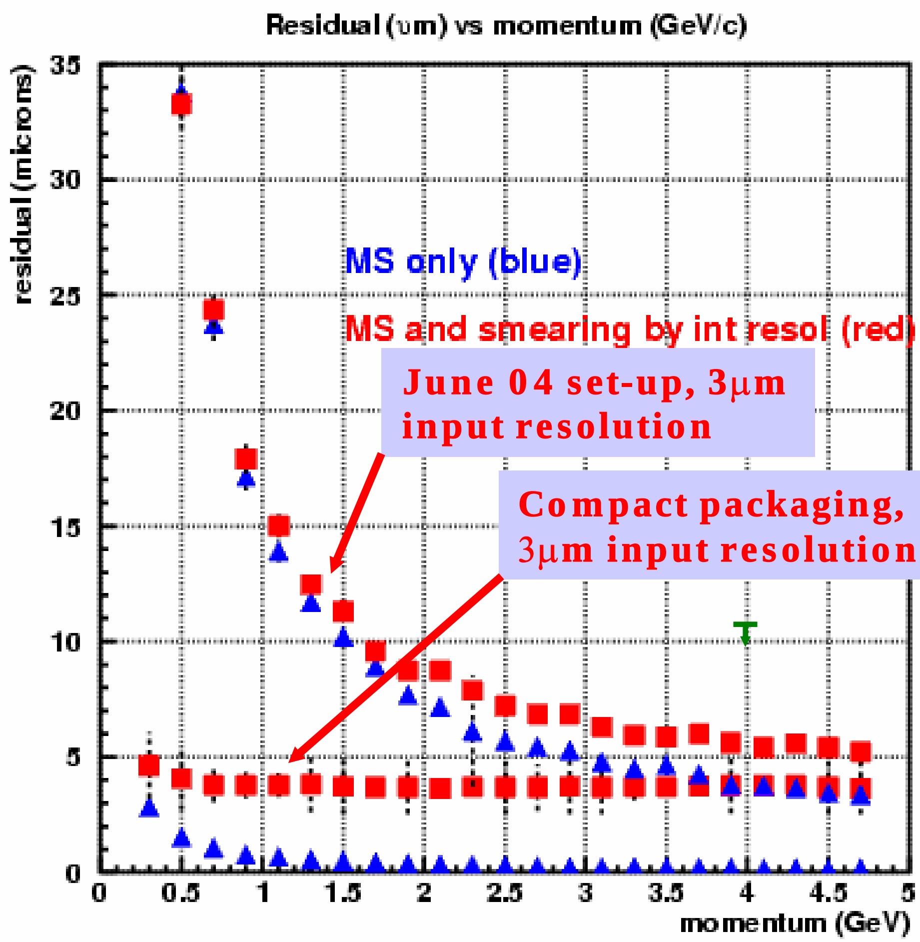
- **Compact packaging for next beam test:**
  - **Expect a better upper limit on intrinsic resolution**





Highlights: - **<0.3cm between CAPS.**
- **reduced material**
- **eases alignment.**

Hit resolution (GEANT simulations)



12µm/20µm IR for strips

@ 4GeV, 5-7µm (as in June beam test configuration) → 4µm

Effects of multiple scattering and of distances become negligible!

Looking forward to next beam test

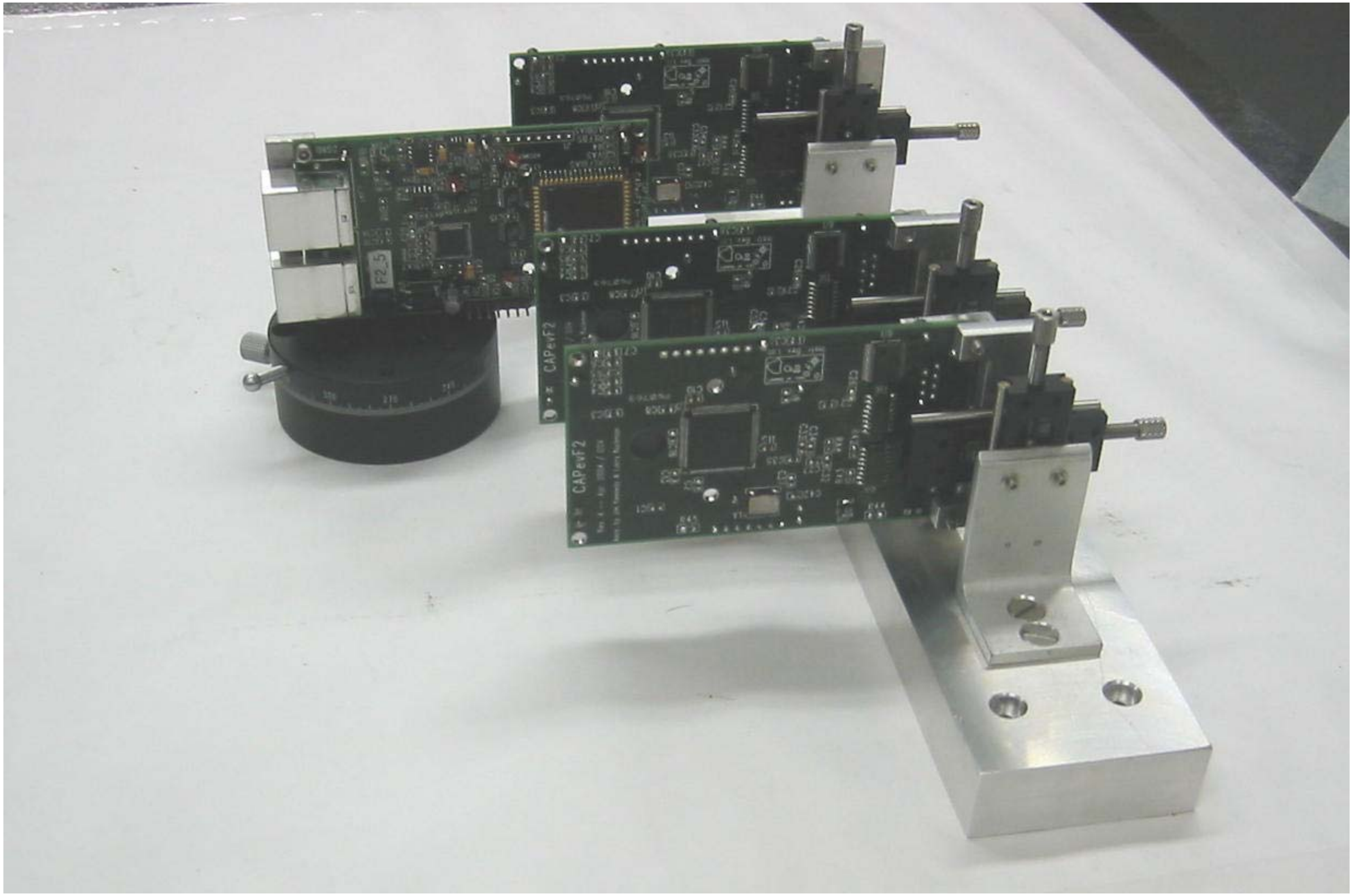
Highlights & Conclusion

MAPS is a promising technology for a Super-B Factory.

- **Successful beam test in June:**
  - **Experience gained / Demonstrate beam test operation.**
  - **UL on IR: 11μm / Charge spread: 90% in 4 pixels.**
- **CAP2 and next iterations:**
  - **Works alright, more work to be done → improvements.**
- **Further Radiation Damage Studies:**
  - **Still a hot topic but positive preliminary studies, we wait for new data points.**
  - **Demonstrate operation with highly irradiated detectors.**

Have started to write down the basis for a future Belle Pixel Vertex Detector 1.0 TDR.

Back up slides



Next CAP designs

- **New CAP prototype designs:**
  - **CAP3: "prototype iteration"**
    - **- Array same size, might be larger.**
    - **- Go from 0.35 μm to 0.25 μm process.**
      - → **From 4 to 5 metal layers: better shielding!?**
      - → **Increased radiation-hardness(?)**
      - → **More pipeline if possible.**
      - → **Technical change in pipeline: less dispersion.**
      - → **Differential reads!? (might be tricky to implement)**
  - **CAP4: "full-size detector"**

CAP4:

Interests: experience with full-size MAPS , realistic constraints on system architecture ,.

Disadvantages: risky as it costs ¥¥¥ / $$$ (CAP4 ~7.5X more expensive).

System architecture

- **System architecture:**
  - **A topic we are now actively investigating:**

    Four system architectures considered at present time, number might increase:

    a) High speed analog buffering.

    b) High speed analog buffering with on-chip data reduction.

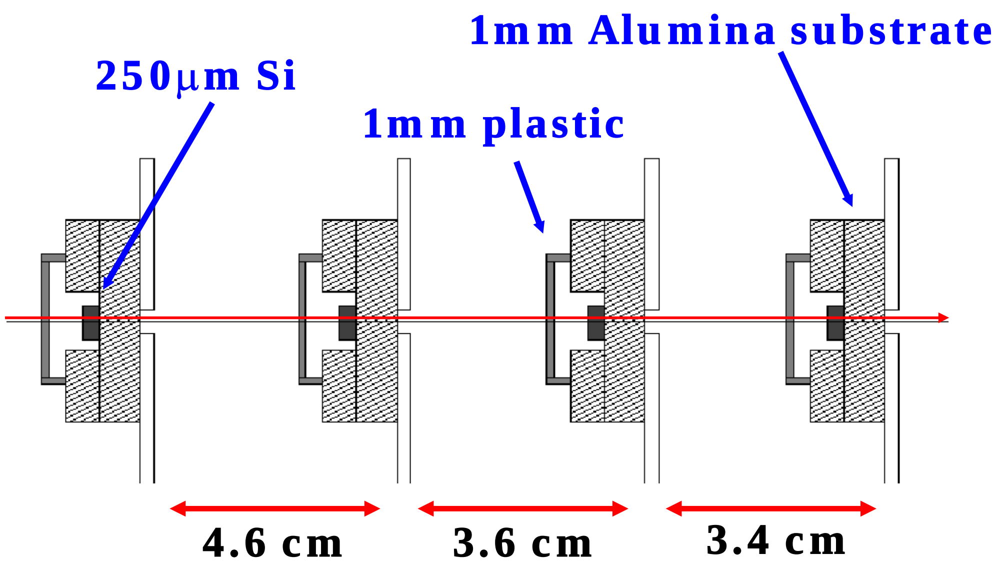
    c) ADC on Front-End board and (sparsified) digital data transfer.

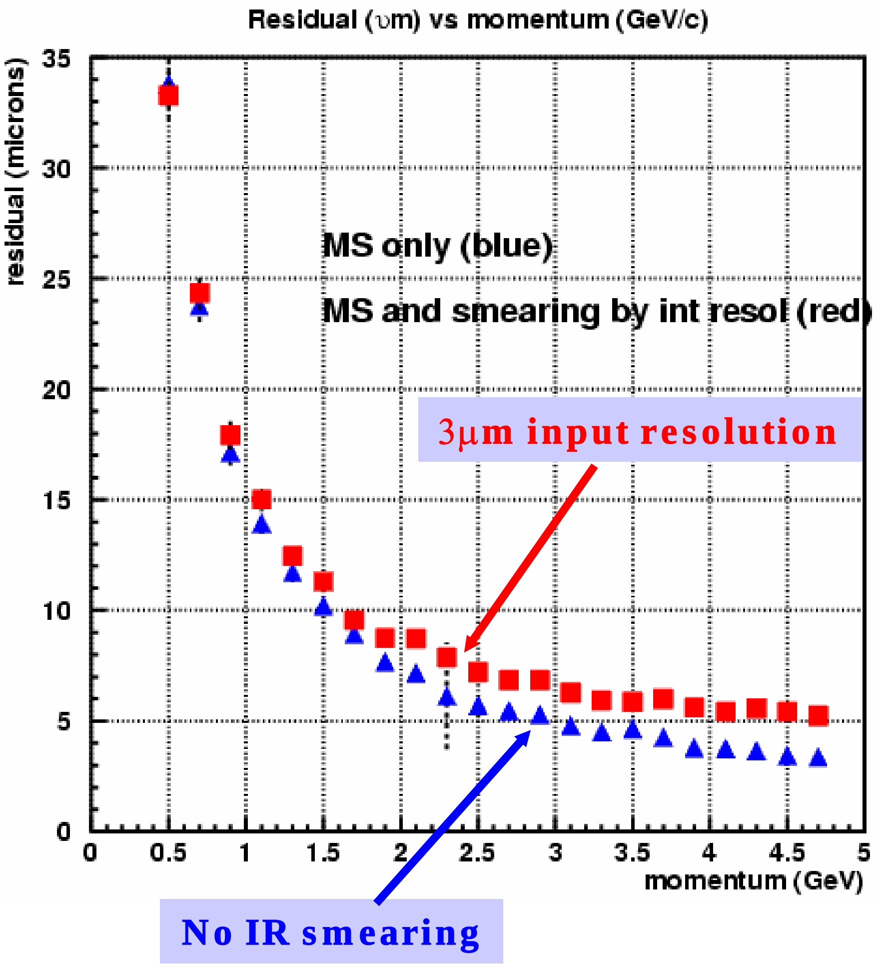
    d) Digital pulse width modulation.

    → Estimate data volumes vs. system architecture.

    → Link to the Data Acquisition system of Belle.

Resolution: GEANT Expectation





In our case: measurement of intrinsic resolution degrades mainly because of distances between pixel detectors (constraints from Front-End board design)

Vertex Detector @ S-Belle

→ **Detector must tolerate increased hit density and large radiation doses.**

- **Occupancy**

  Current robustness is marginal. At 20x background, even with segmentation ("striplet") and shorter shaping/pipelined readout – a concern

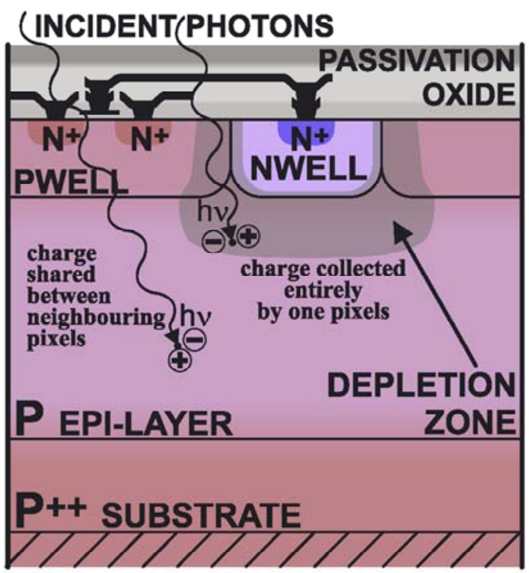
- **Improvement**

  One of the few areas in which the detector can be improved

Recent advances in deep sub-micron MAPS look promising for S-Belle vertexing.

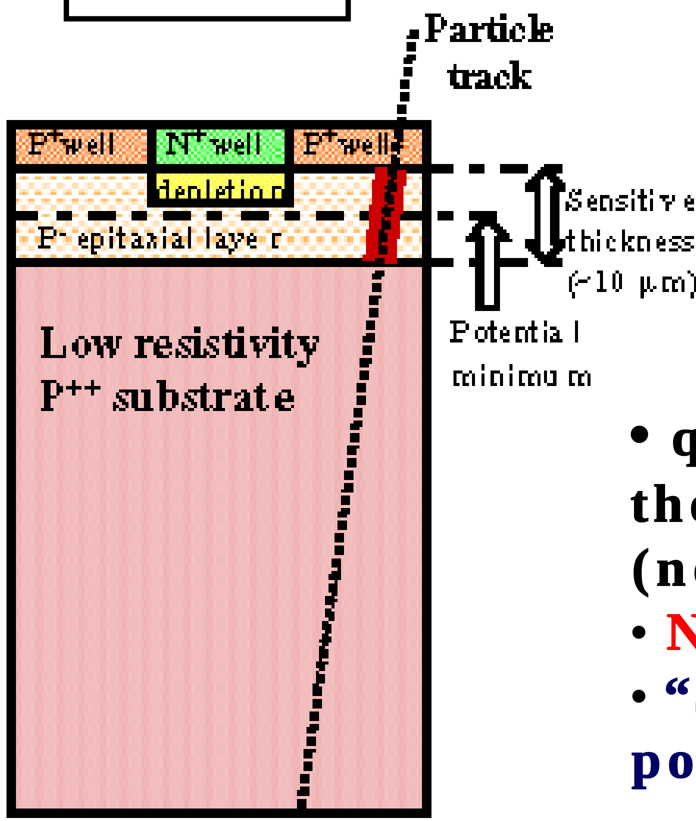
Basic Technology: Standard CMOS

CMOS Camera



Because of large Capacitance, need Thick DSSDs -- APS can be VERY Thin

Particle Detector



Standard CMOS:

- Low Power
- Excellent Transistors
- Tight Process Control
- Excellent Uniformity
- High volume, low cost
- Large ADC, DSP base

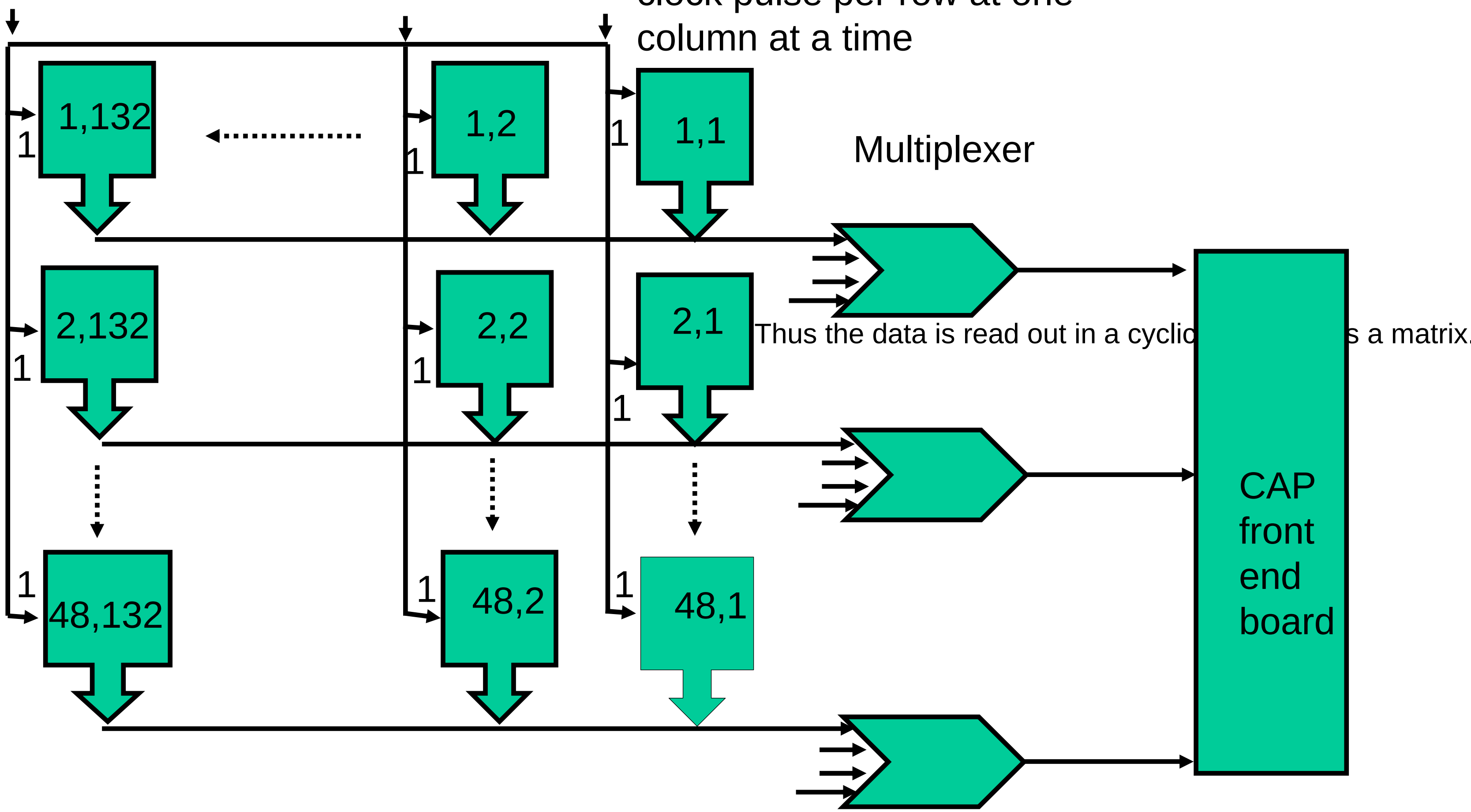
Key Features:

- q collection via thermal diffusion (no HV)
- NO bump bonding
- "System on Chip" possible

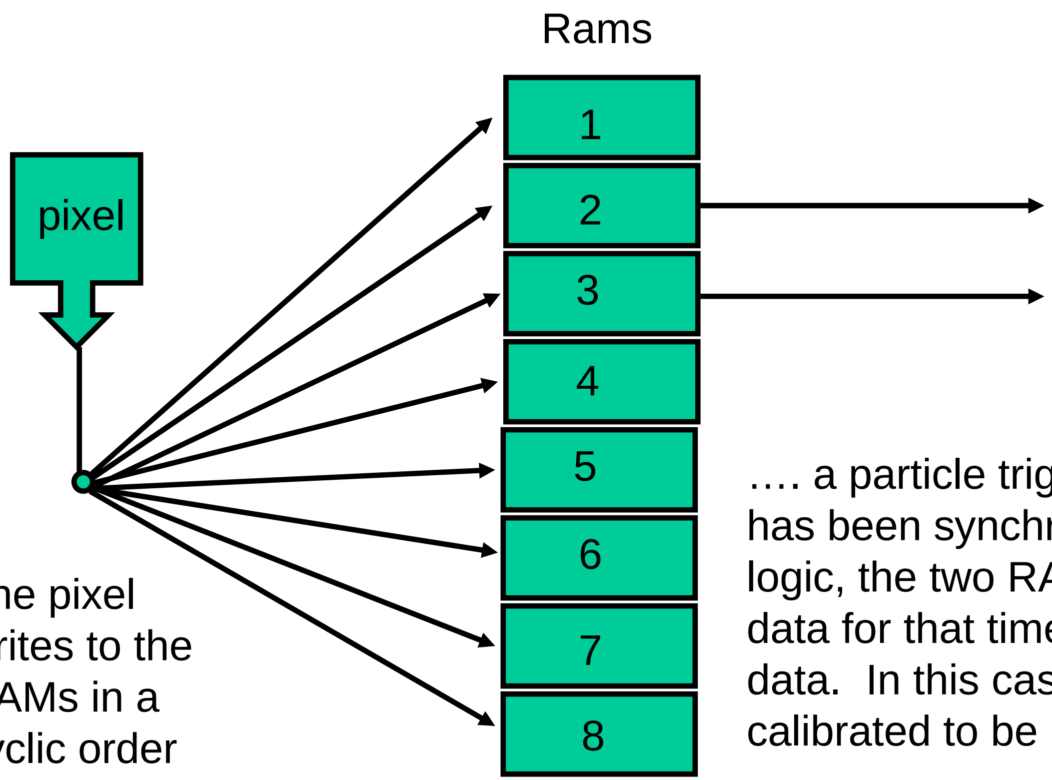
The CAP1 process

How the CAP1 works and reads the data.

Sends a read "1" down at clock pulse per row at one column at a time



The CAP2 Process

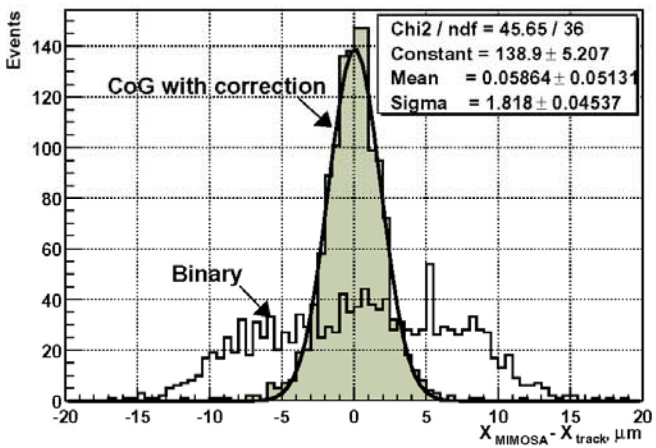


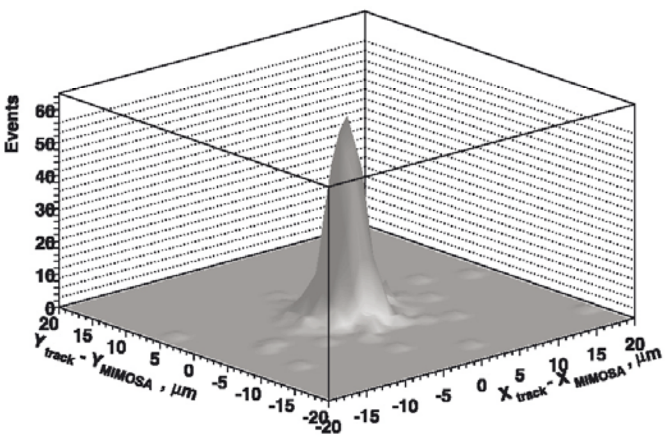
The pixel writes to the RAMs in a cyclic order until…

…. a particle triggers the PMT, which has been synchronized with the CAP logic, the two RAMs that have the data for that time period ship out their data. In this case, say at a time calibrated to be between RAMs 2 & 3.

Promising Results

CMOS MAPS particle tracking performance (20 μm pitch)





ENC ~10 electrons: S/N>30
Efficiency (5σ seed cut): ε_{MIP} > 99 %
Spatial resolution: σ = 1.4 μm

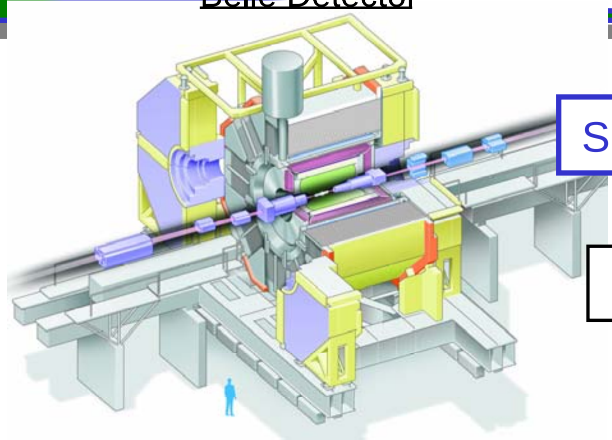
Demonstrated on several devices in various submicron CMOS processes:

AMS 0.6 μm, 14 μm epi
Alcatel 0.35 μm, 4 μm api
AMS 0.35 μm, no(!) epi
…
TSMC 0.25 μm, 8 μm epi
(LBL team)

+UH, RAL, …

Development Efforts

Belle Detector

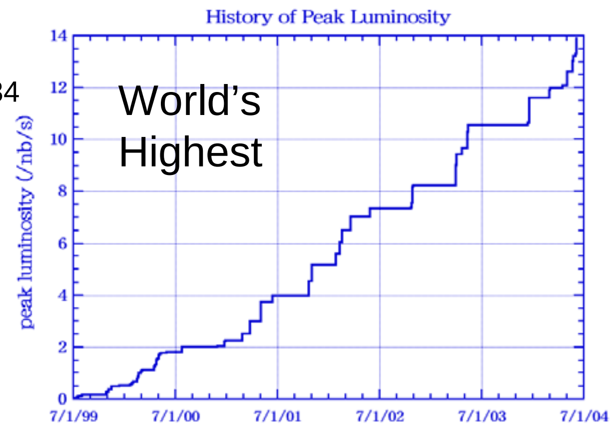


Super-Belle: <=10μs

See T. Tsuboyama's talk

L=10^{34}

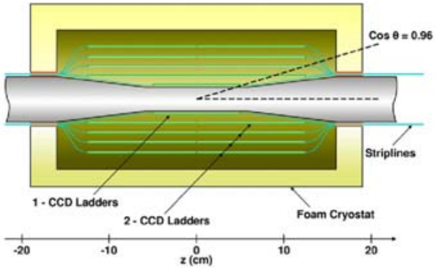
World's Highest

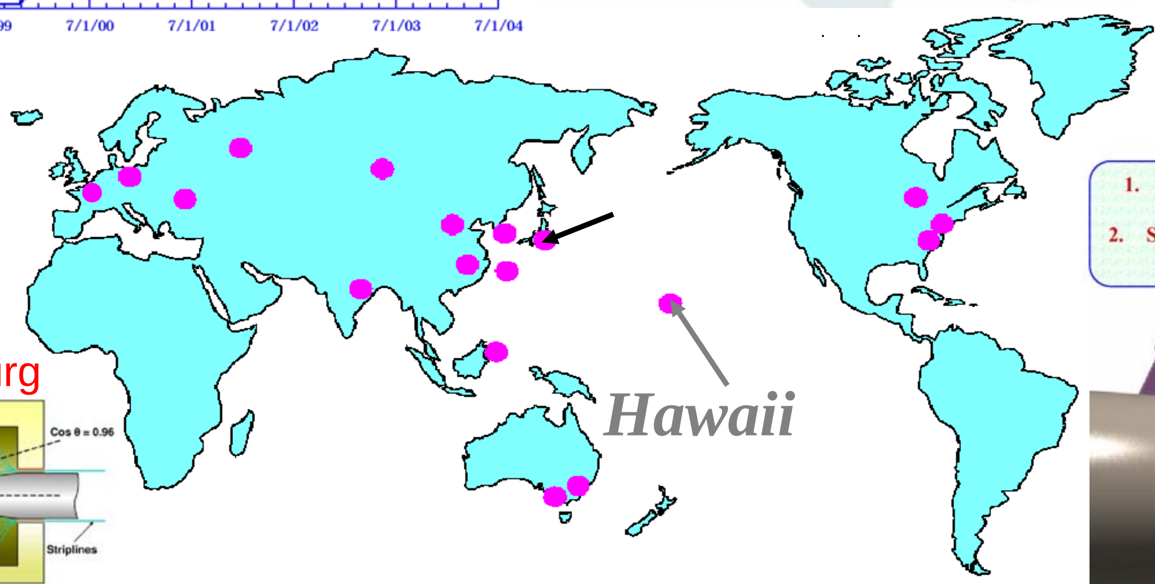


LEPSI, RAL, Strasbourg

Linear Collider

DESY/Hamburg

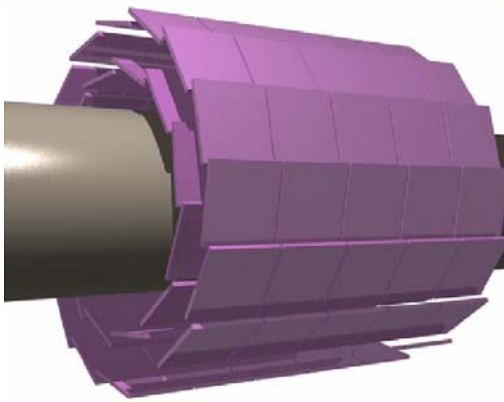




LBNL, UC Irvine

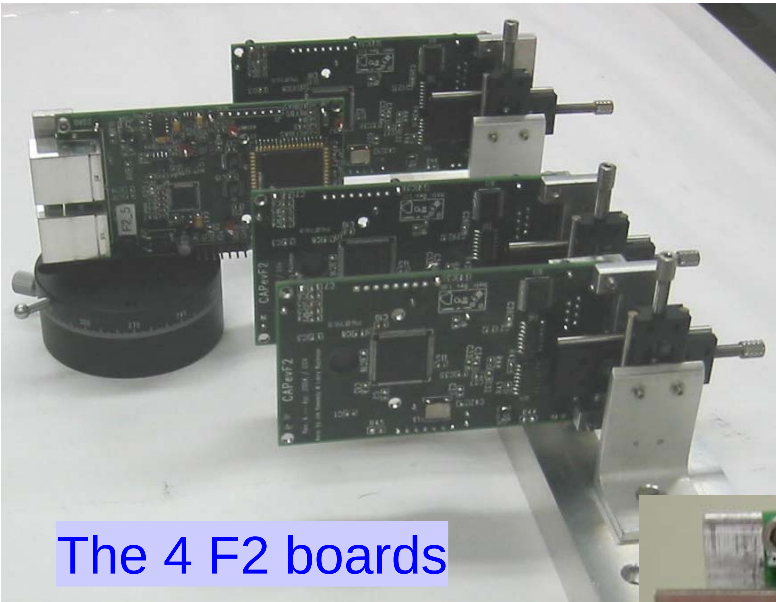
STAR μvertex detector

1. First upgrade (x4 present luminosity, 2006): 10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008): 2 – 5 ms readout (integration) time



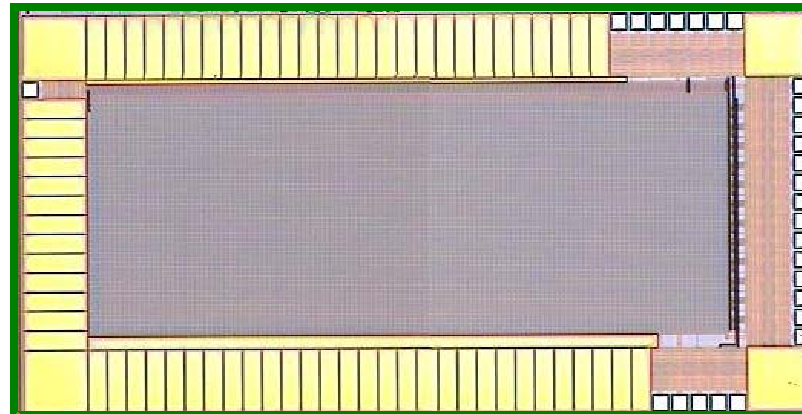
Apologies to those not mentioned:
Easy access will bring others

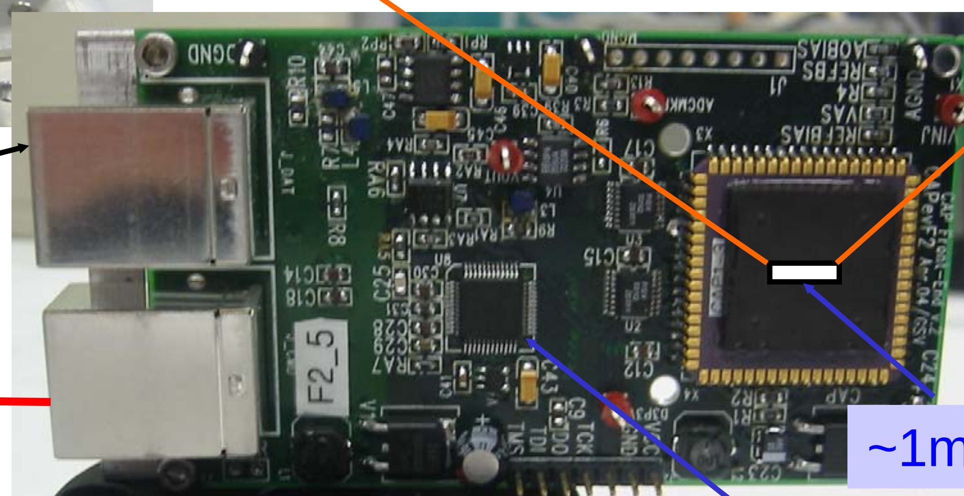
Example of Ease of Use



The 4 F2 boards

Pixel chip: 132x48=6336 channels





All LVDS digital I/O

300-600Mbaud link

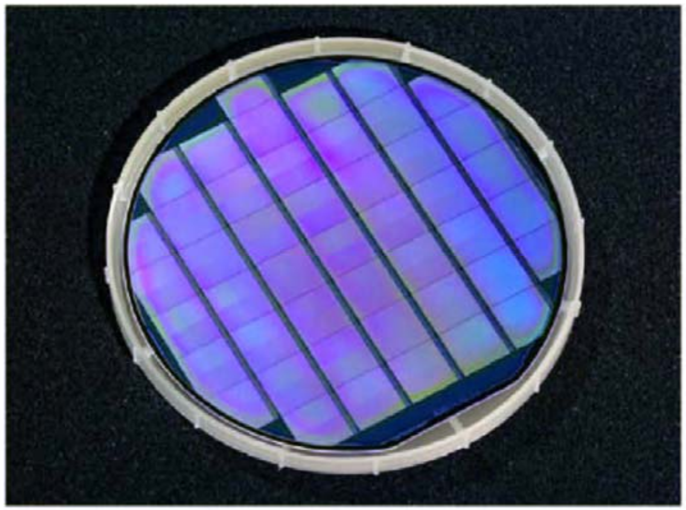
~1mm x 3mm

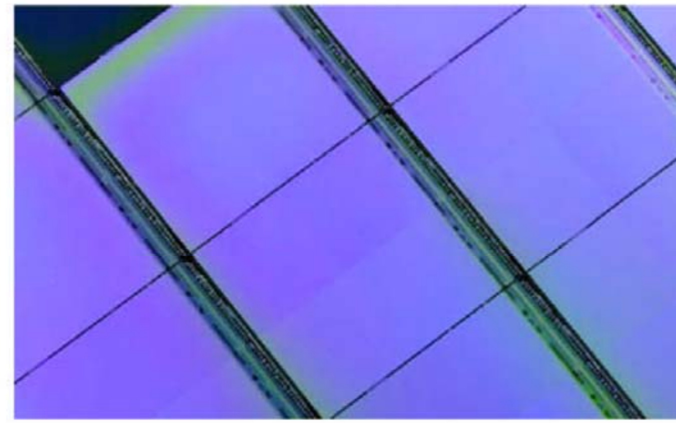
On board ADC

Critical R&D Items

1. Rea
   1. ST
   2. N
2. Rad
   1. ST
   2. Su
3. Thi
4. Full

MAPS wafer scale prototype: Mimosa 5

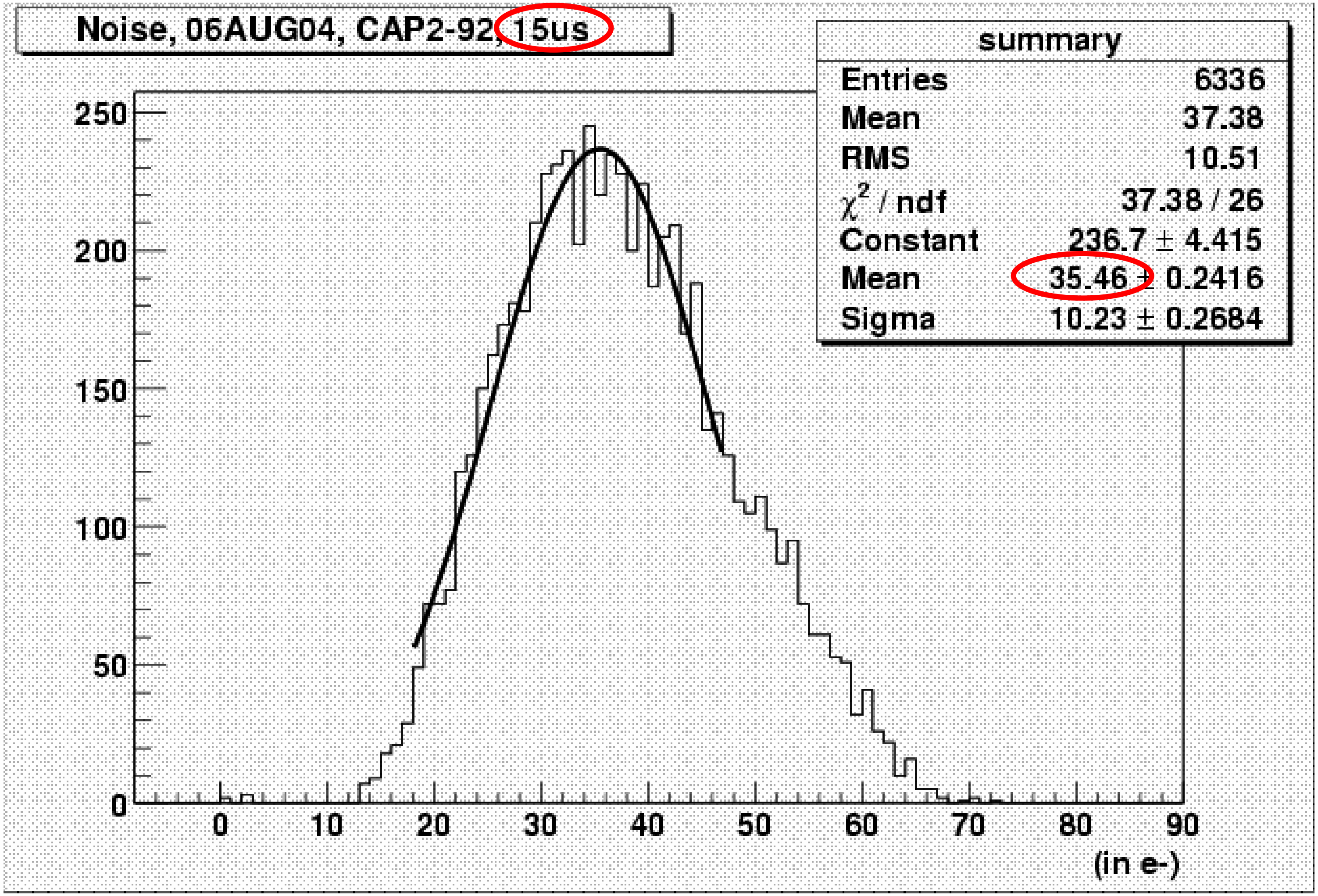




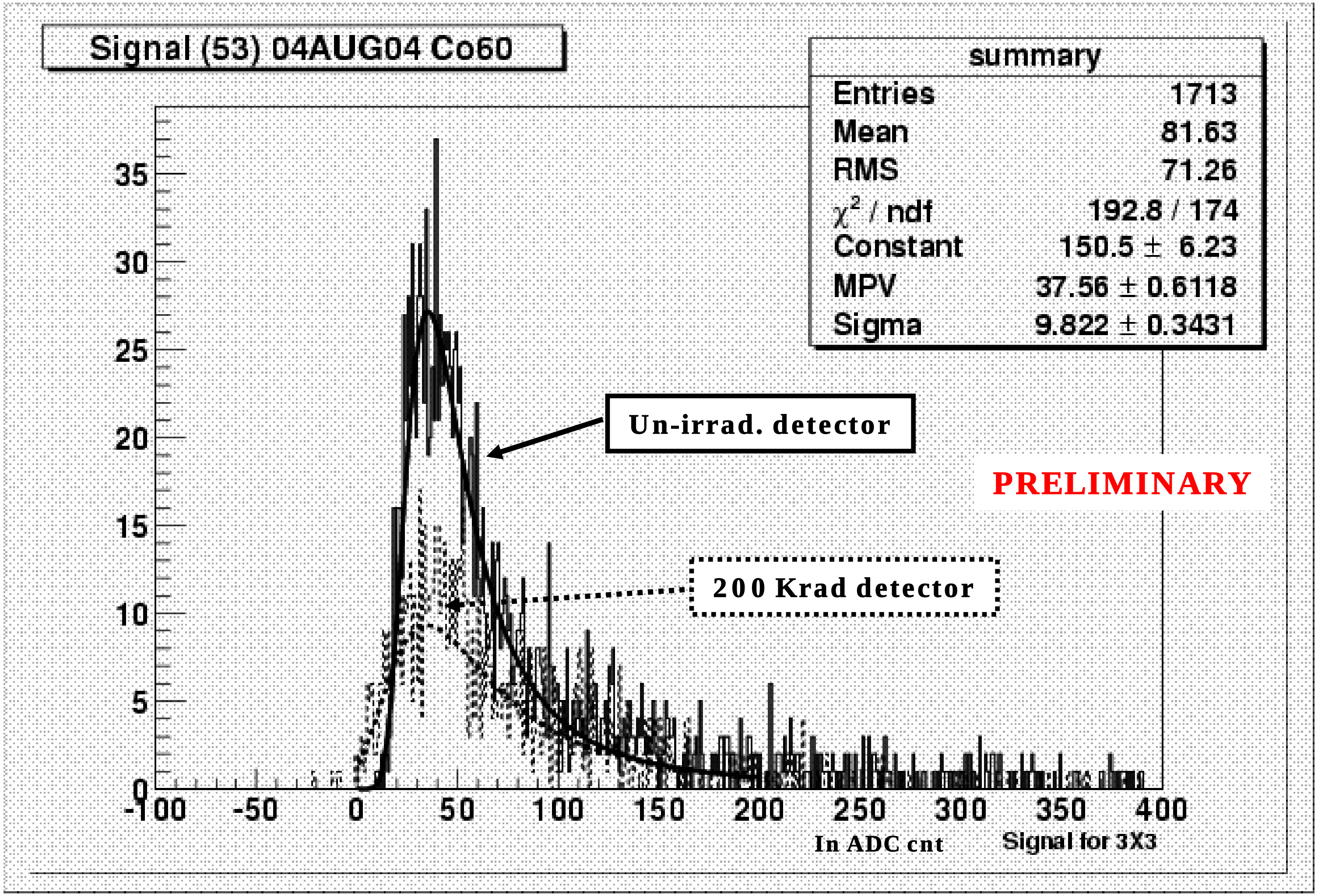
Mimosa-5 status

- 6 wafers delivered by AMS
- 3 wafer back-thinned (down to 120μm) and sliced
- prober tests of all wafers in progress: first estimation of yield ~30%
- beam tests at CERN: results as expected
- fine back-thinning tests at CNM Barcelona and ITE Warsow

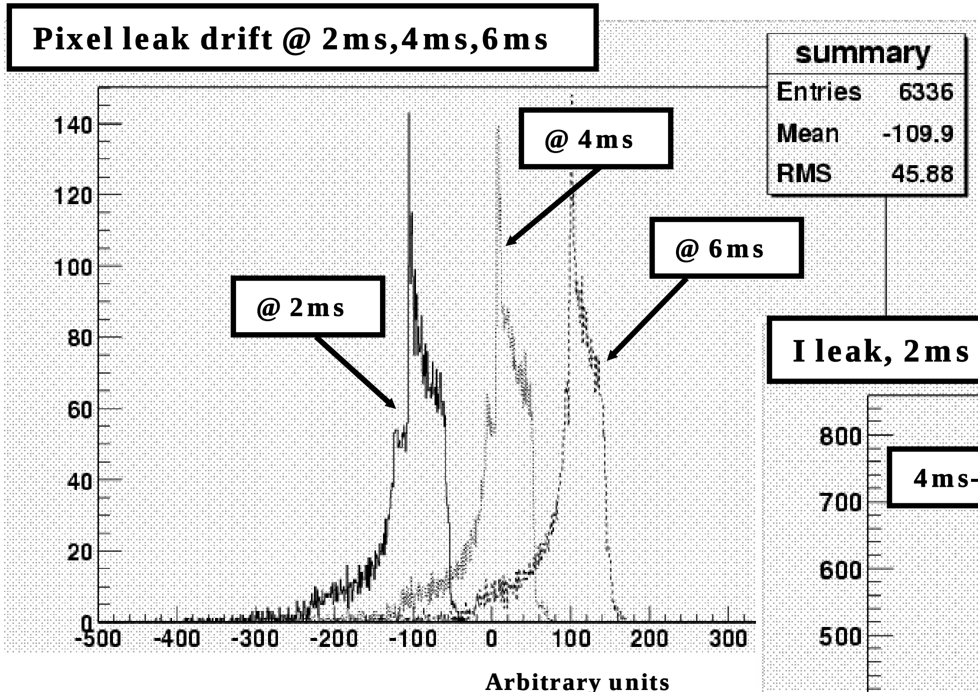
CAP2 noise as of 06AUG04



200Krad vs. un-irrad. C060

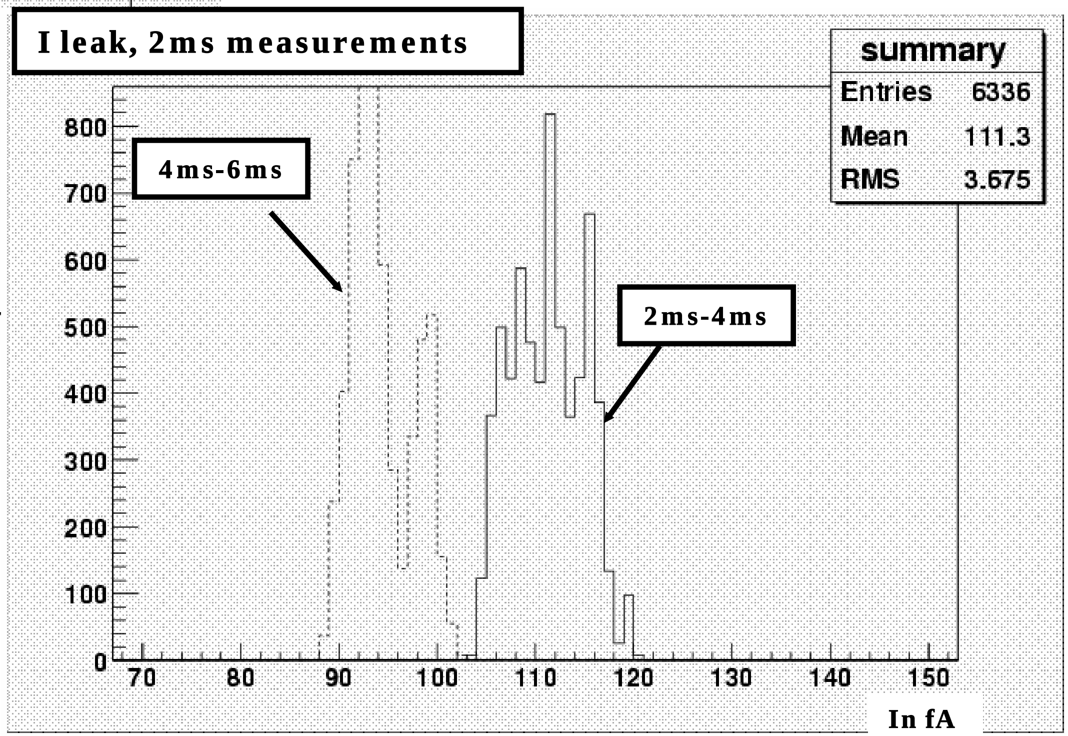


I Leakage 2Mrad annealed



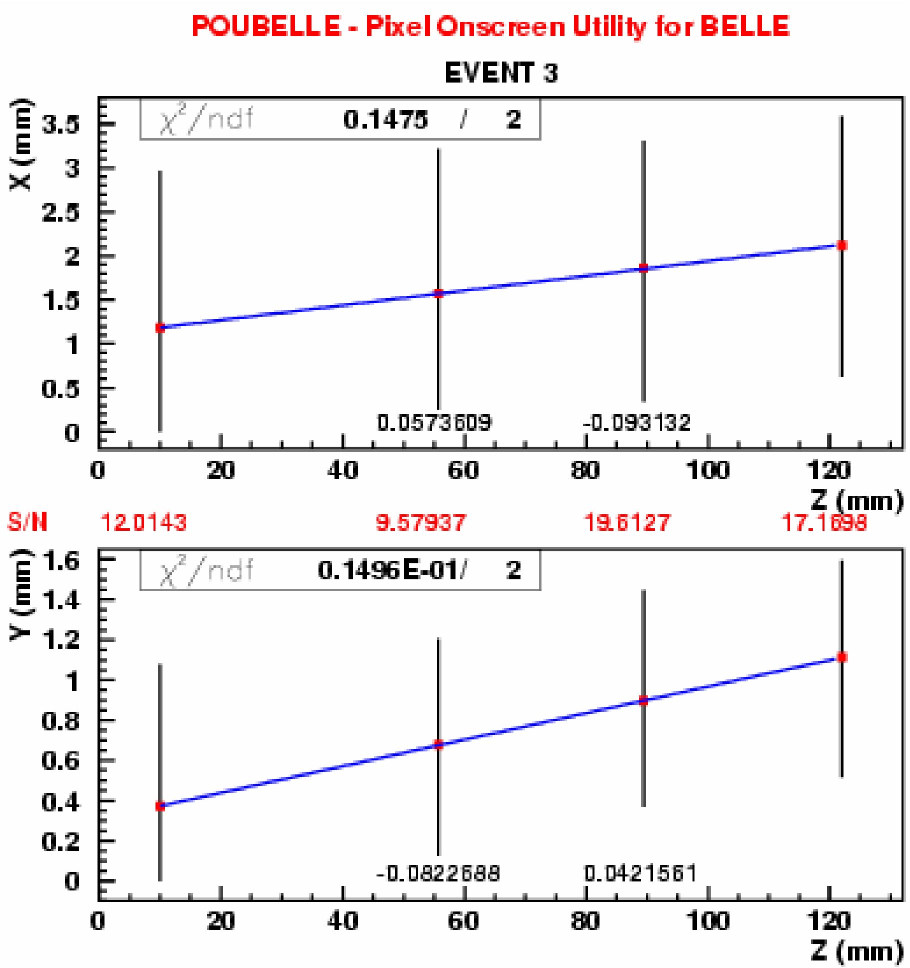
For 2Mrad detector annealed: 60hr/60C & 2mo/20C.

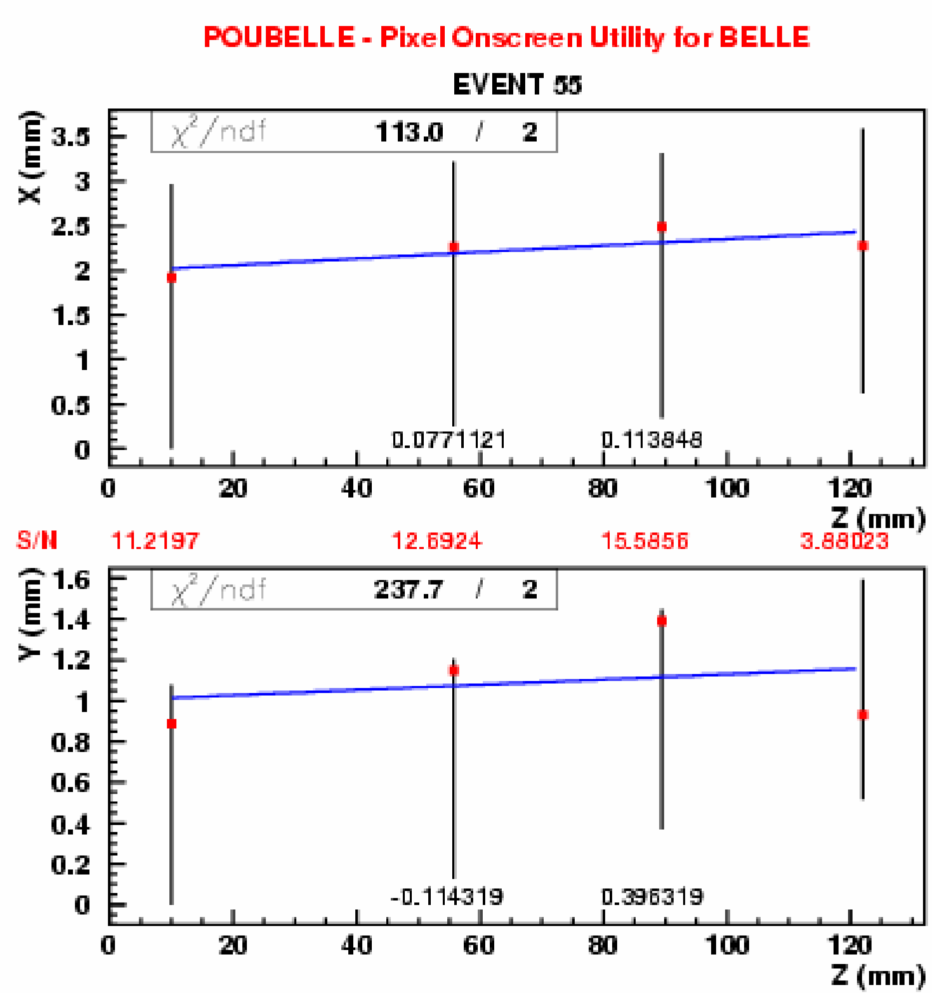
03AUG04



Estimate thus Ileak ~ 111 fA

Track Fitting / Residuals





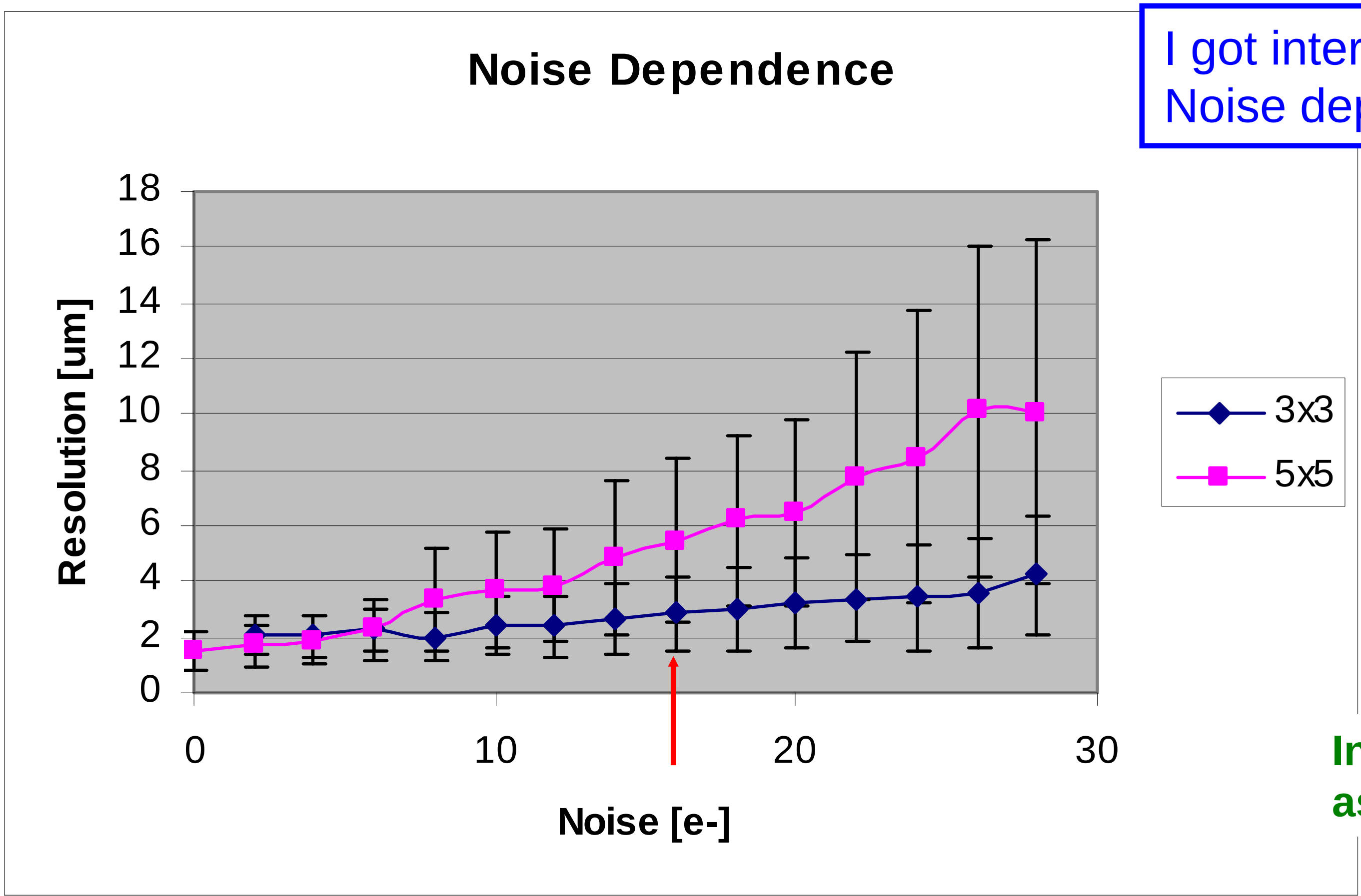
Required Transfer Rates

- CAP1 architecture (if 10μs max. latency):
  - 15mm radius:
    - 67 Gpixels/s
    - ~1Gpixel/s/pin
  - 10mm radius
    - 39 Gpixels/s
    - ~0.5Gpixel/s/pin
- CAP2 architecture (>= 100μs max. latency):
  - 15mm radius:
    - 6.7 Gpixels/s
    - ~100Mpixel/s/pin
  - 10mm radius
    - 3.9 Gpixels/s
    - ~50Mpixel/s/pin

Two ways around:
- Multi-orbit
- "Tiling"

Real max. latency
Set by <L1/L2> rate

Toy Monte Carlo



I got interested in the issue of Noise dependence

- random hits
- diffusion simulation:
  - substrate loss
  - recombination
  - add noise
- reconstruct track using c.o.g. and compare

Intrinsic could be as good as 3um:

Alignment errors and multiple-scattering will likely dominate