Pixel Detector Upgrade Progress

Belle Pixel Group
Monday Meeting Update
20 Mar 06

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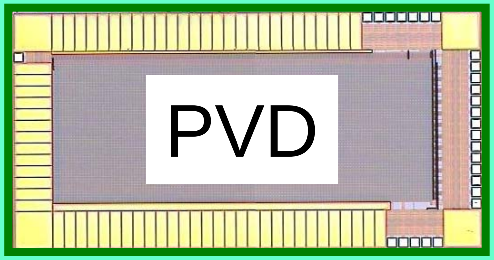


Today's Agenda

- Current Pixel Prototype (CAP3) Results
  - Problems, limitations and lessons learned
- Plans for next CAP detector steps
  - Prototype design concepts and schedule
- PID Upgrade Readout
  - 2x New ASIC prototypes in fabrication

Pixel Upgrade Roadmap

Technology Choice

- Fine-pitch bump bonding is a nightmare
- Custom APS -- difficult

MAPS

CAP1 – basic functionality

- Works well, but too slow

CAP2 – pipelined readout

- Layout problems: poor power distribution
- Higher noise

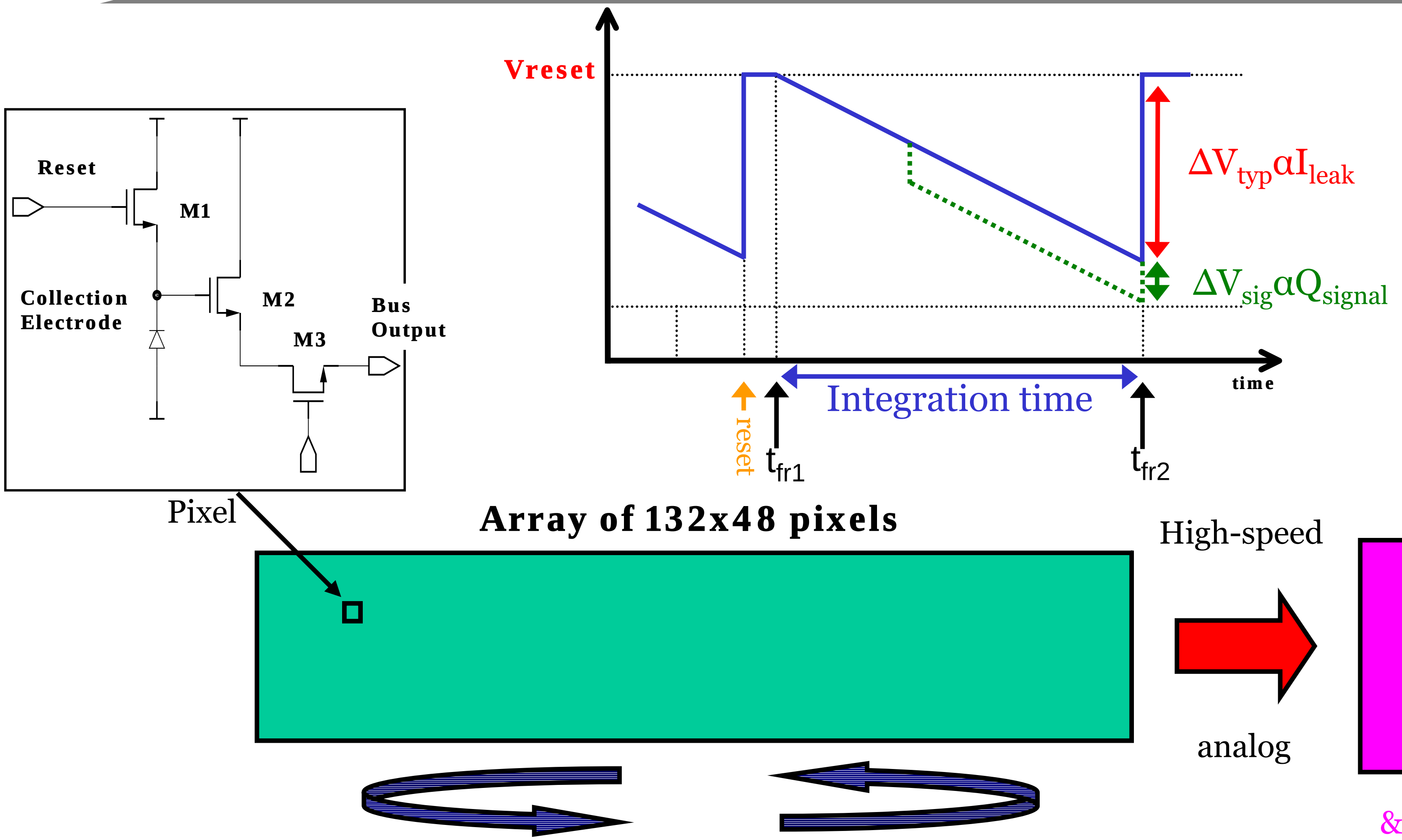
CAP3 – full-size/speed

- Improvements in routing
- Design problems: Too hard to realize readout speed needed

????

More robust, sparsified readout?

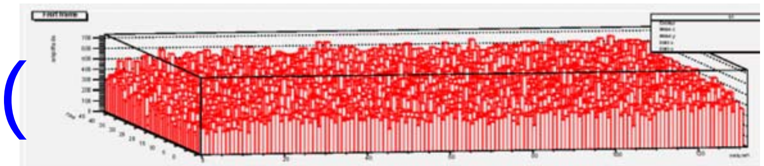
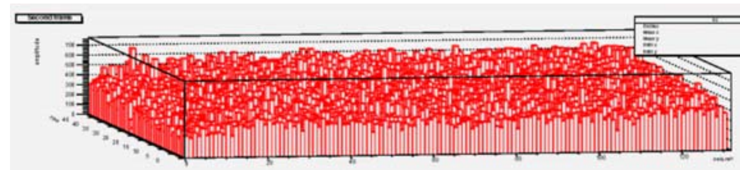
Continuous Acquisition Pixel (CAP)



Pixel Array: Column select – ganged row read

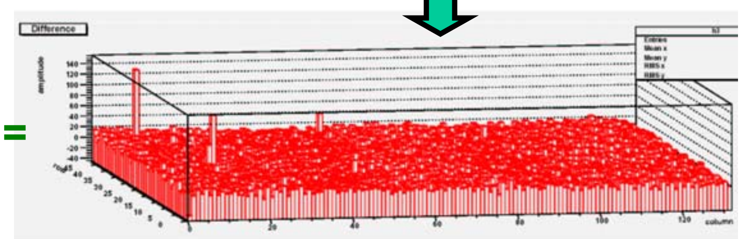
Low power – only significant draw at readout edge

Correlated Double Sampling (CDS)

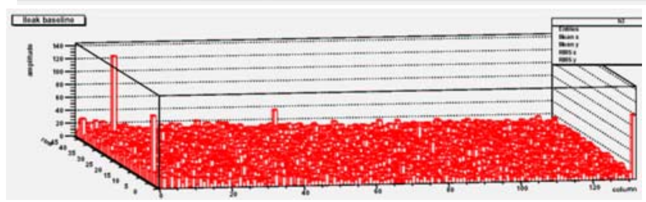
( - )

8ms integration shown

Frame 1 - Frame 2 =

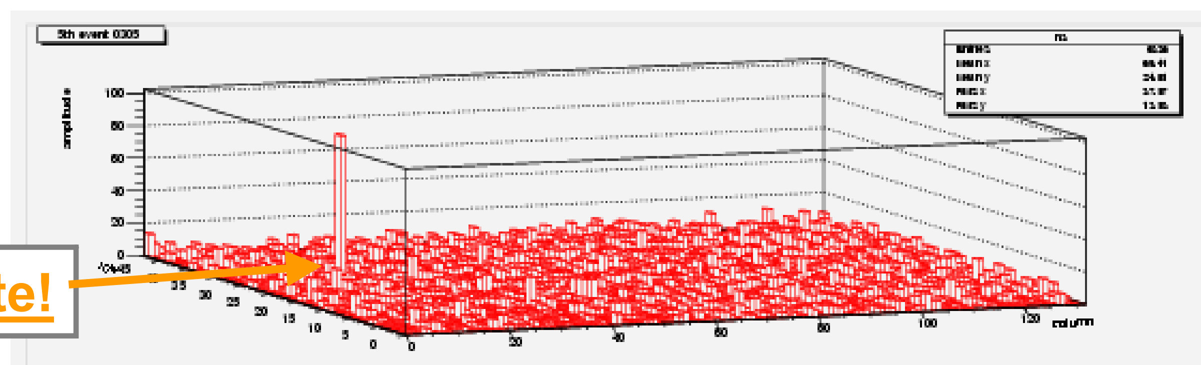


- Leakage current Correction



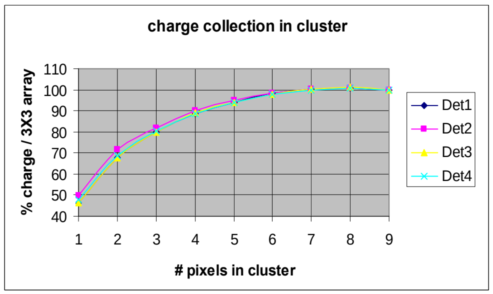
~fA leakage current (typ)
~18fA for hottest pixel shown

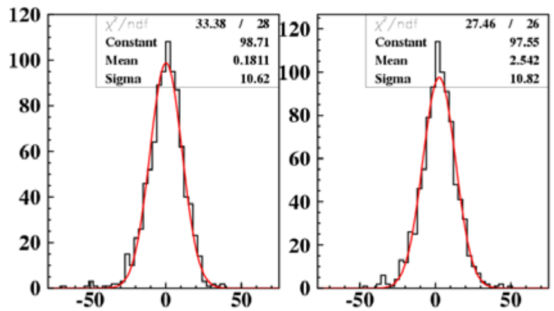
Hit candidate!

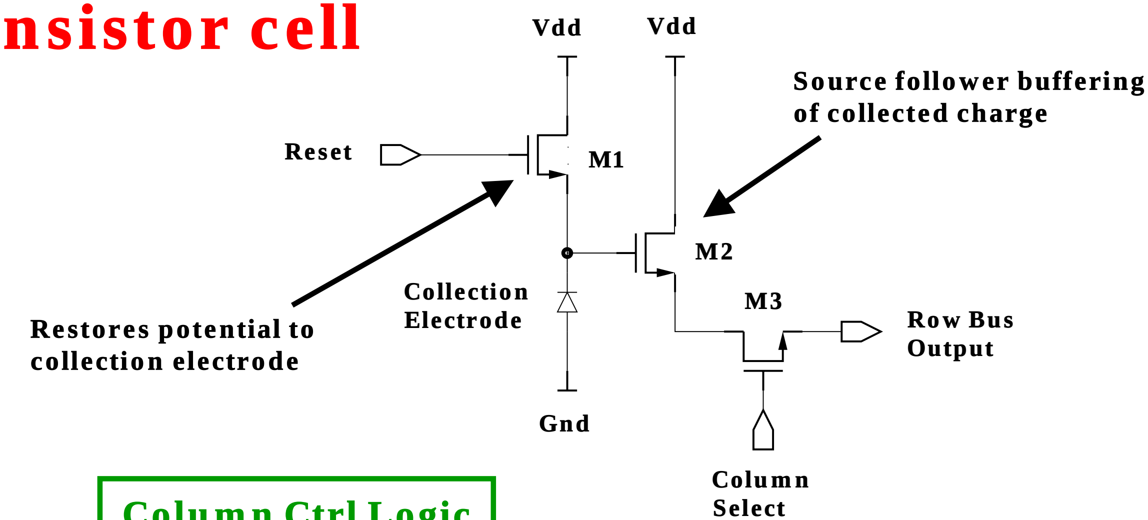


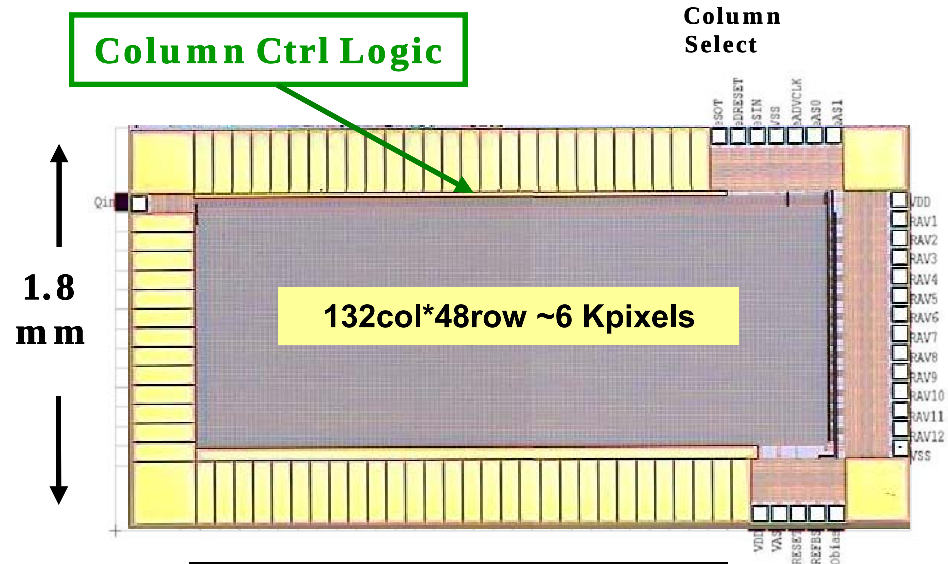
Cont. Acq. Pixels (CAP) 1 Prototype

CAP1: simple 3-transistor cell









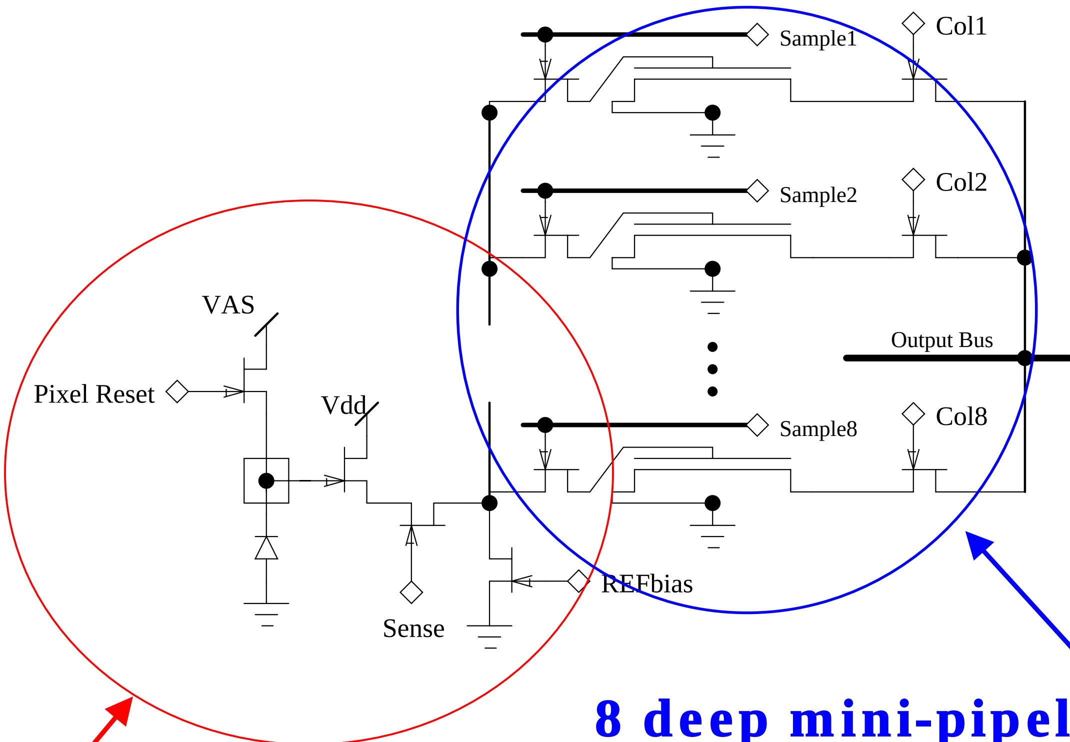
Pixel size:

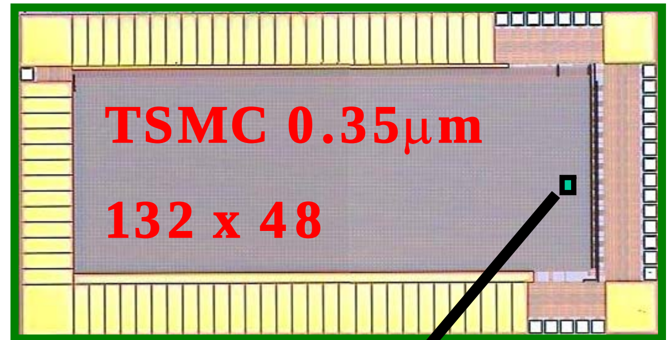
22.5 μm x 22.5 μm

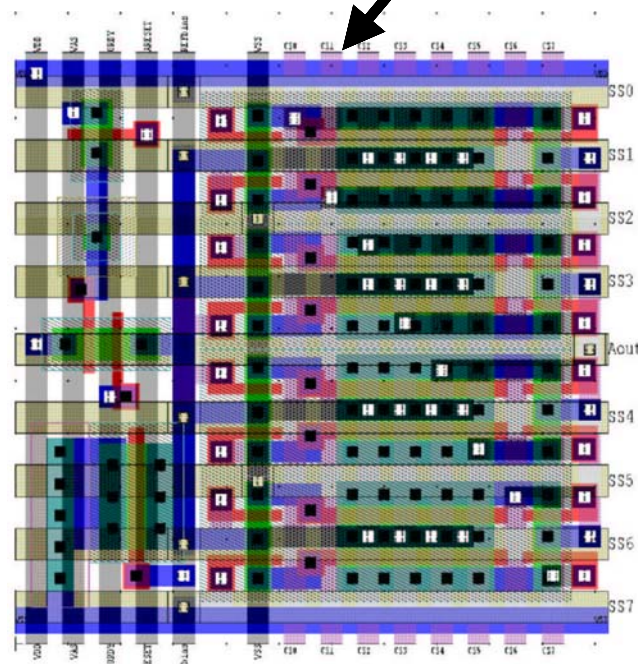
CAPs sample tested: all detectors (>15) function.

NIM A541:166-171 (2005)

CAP2 – Pipelined operation







8 deep mini-pipeline in each cell

3-transistor cell

132x48=6336 channels 50688 samples

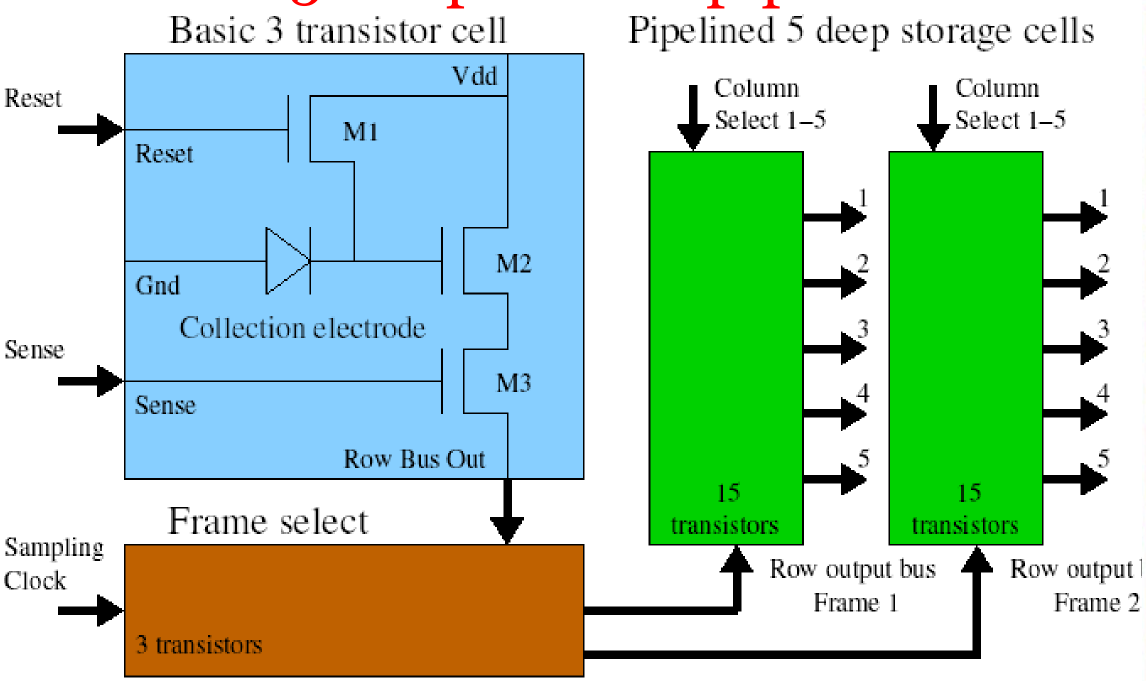
Pixel size 22.5 μm x 22.5 μm

10μs frame acquisition speed achieved!

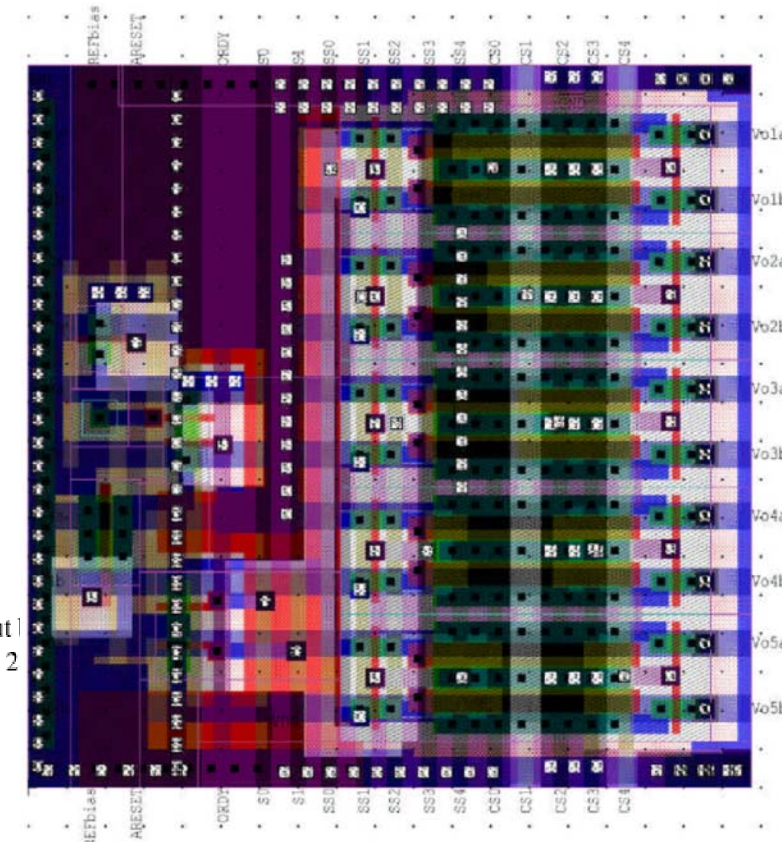
CAP3 – Test Scaling Up (x20)

120Kpixel sensor (128x928 pix)

5-deep double pipeline



TSMC 0.25μm Process



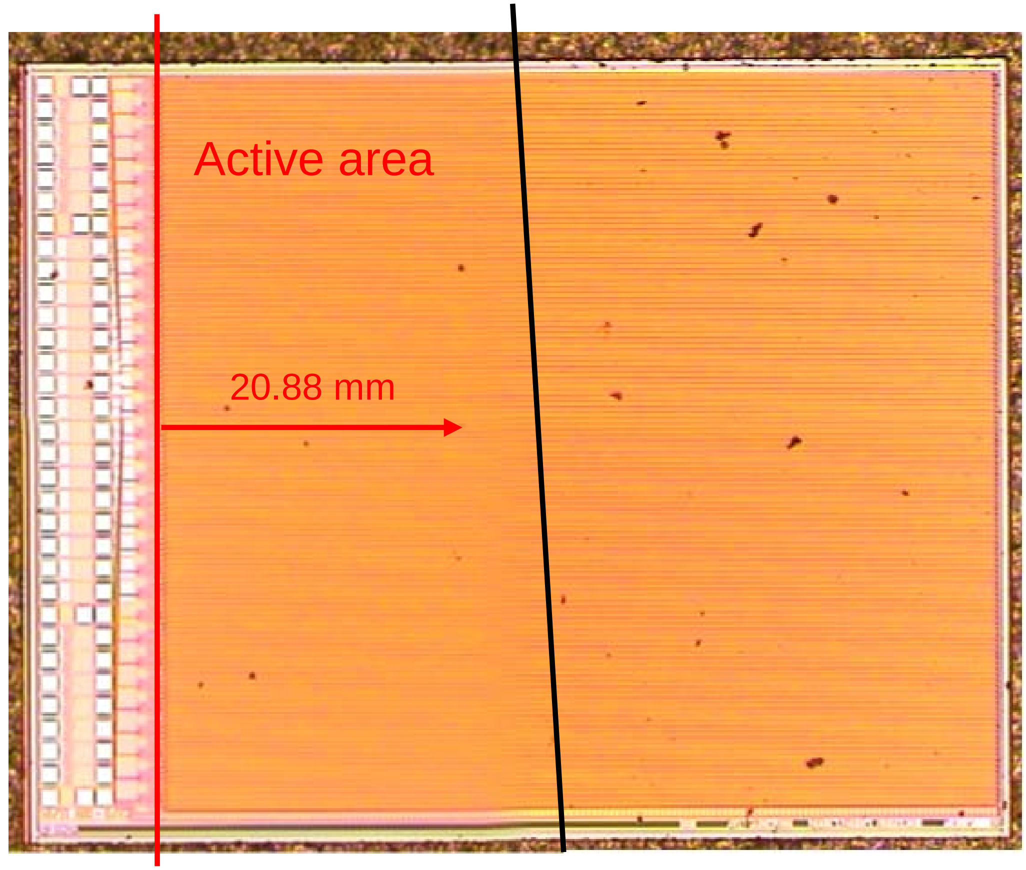
36 transistors/pixel

5 sets CDS pairs

5 metal layers

CAP3 – full-sized!

21 mm



928 x 128 pixels = 118,784

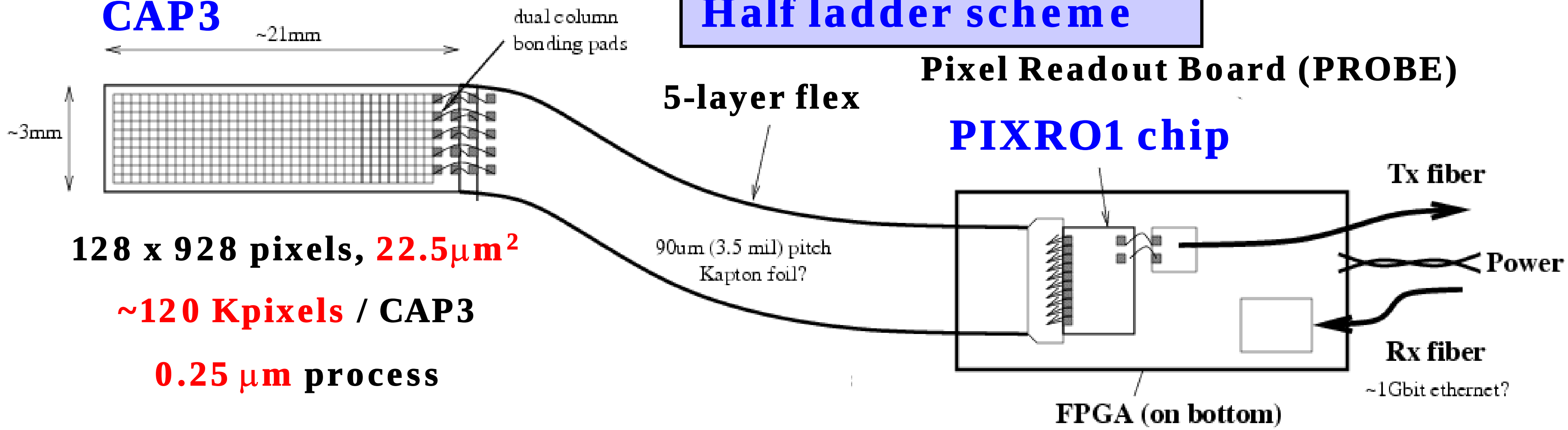
~4.3M transistors

>93% active without active edge processing

CAP3: Full-size Detector

CAP3

Half ladder scheme

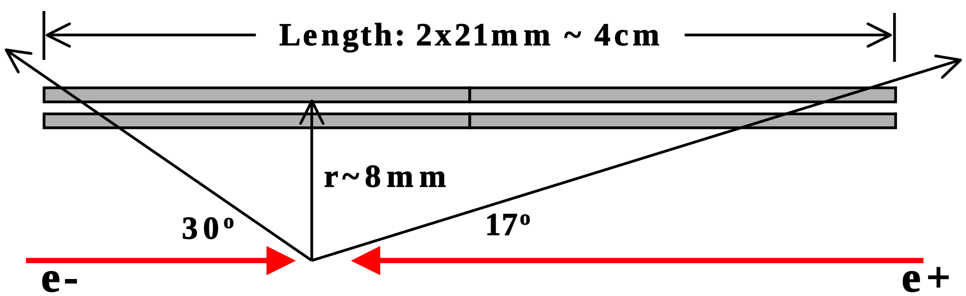


128 x 928 pixels, 22.5μm²

~120 Kpixels / CAP3

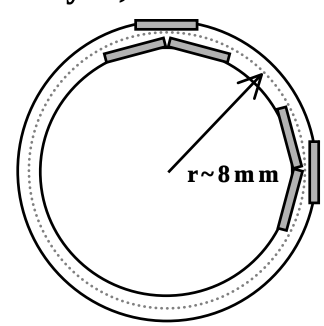
0.25 μm process

Side view



End view

Double layer, offset structure

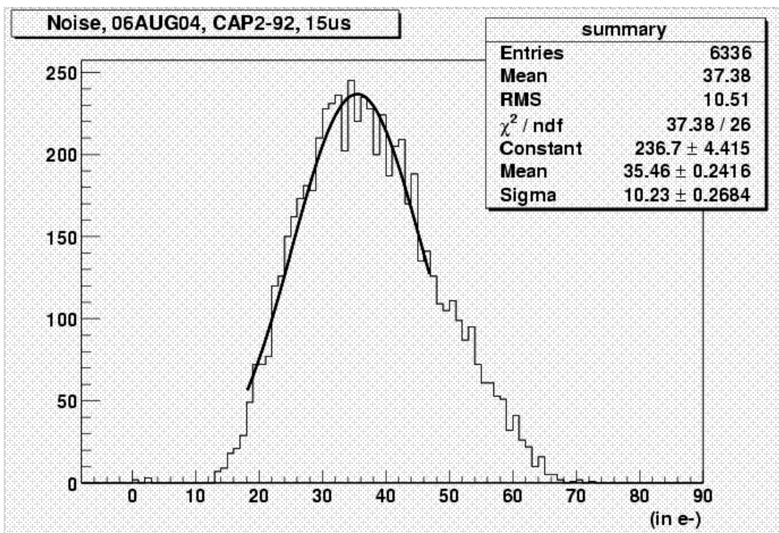


# of Detector / layer ~ 32

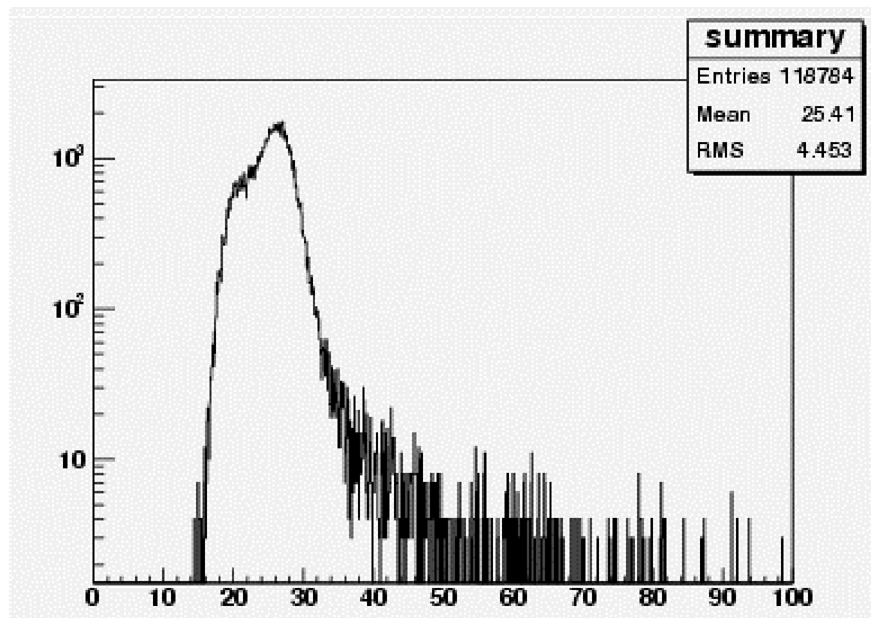
Sounds great, so on to testing…

→Struggled for a long time with

finding Operating point



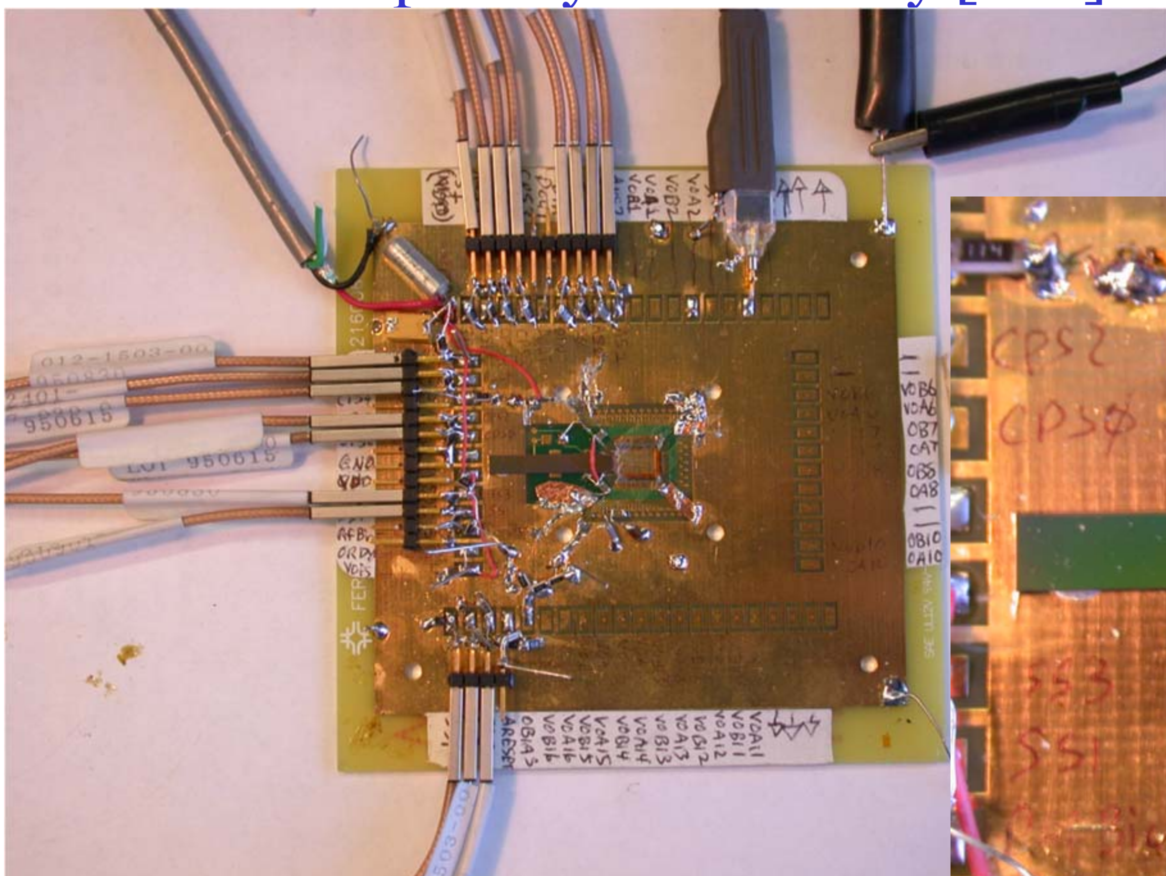
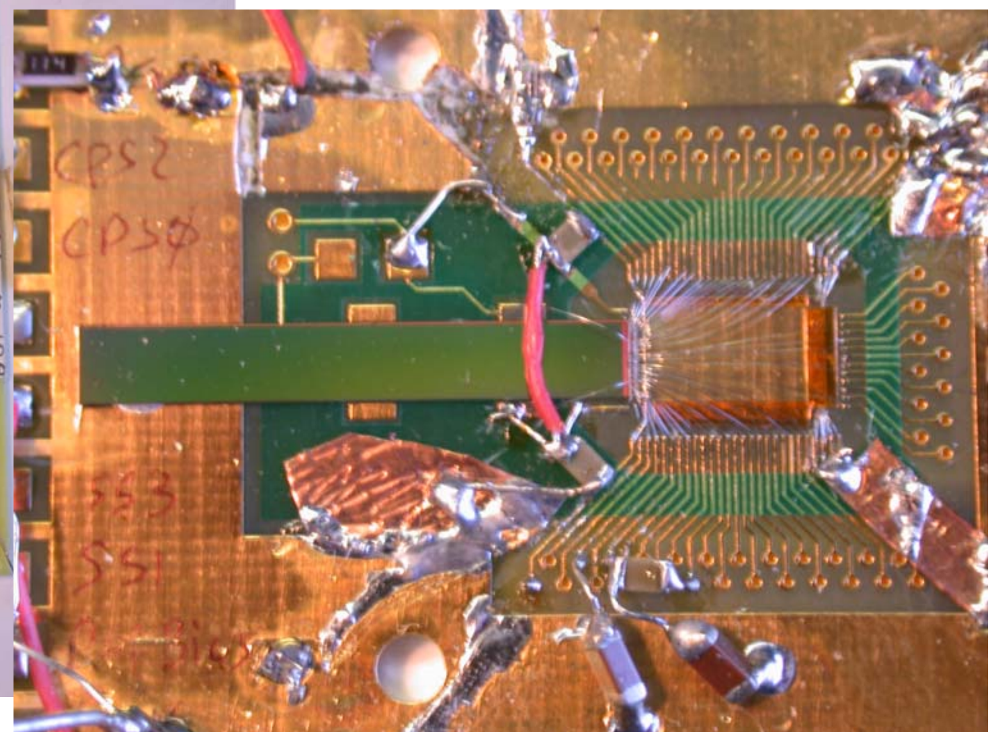
CAP2



CAP3

Test Set-up at Fermilab

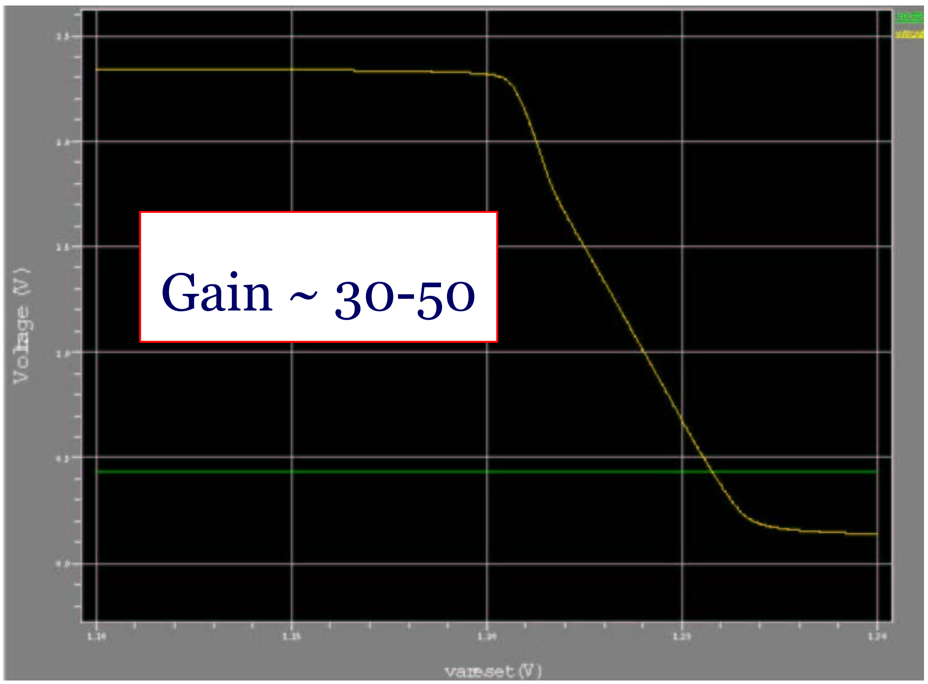
- Tom Zimmerman (ASIC Engineer) visited Hawaii for a couple days in January [ILC]

CAP3 Problems (I)

- Basic storage scheme used in STRAW, LAB1 ASICs, but..
  - Limited dynamic range

Many channels in saturation

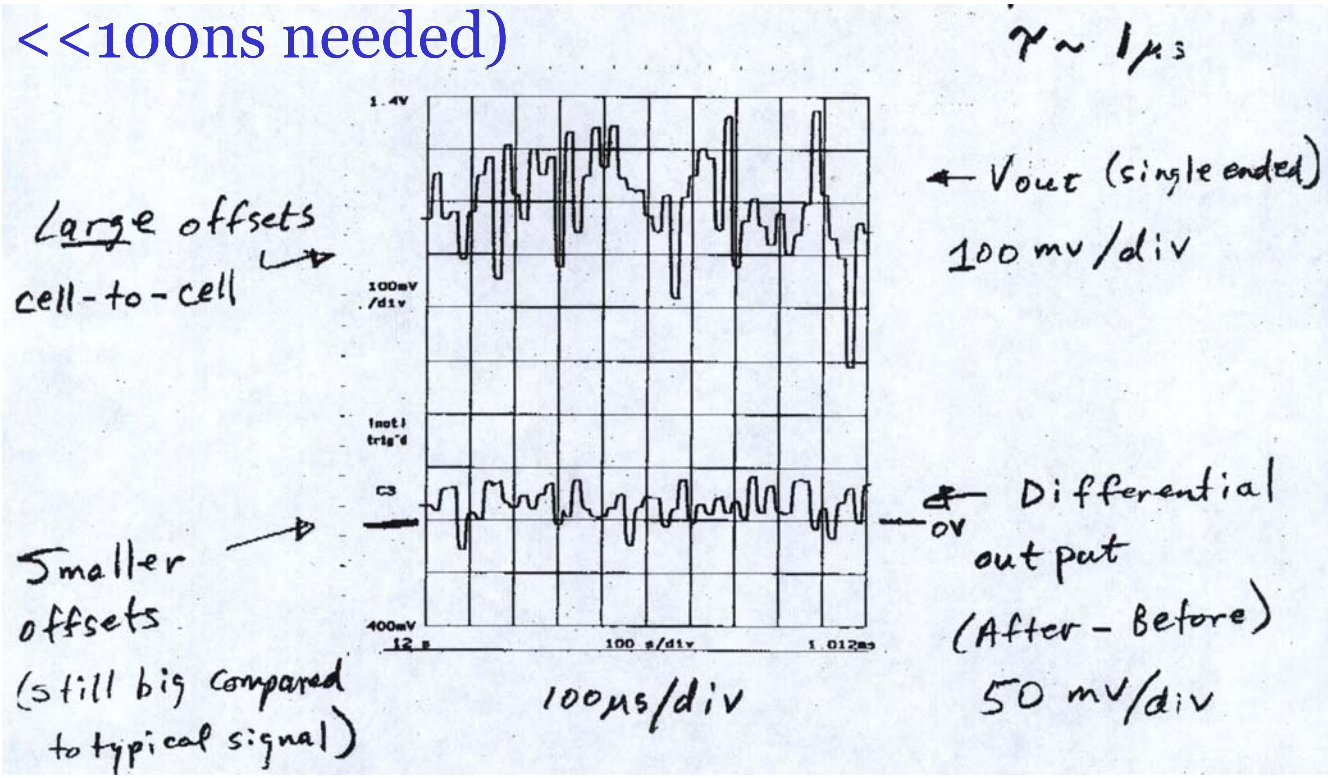


500mV/div

- Poor choice of reset transistor control (shouldn't use VDD)

CAP3 Problems (II)

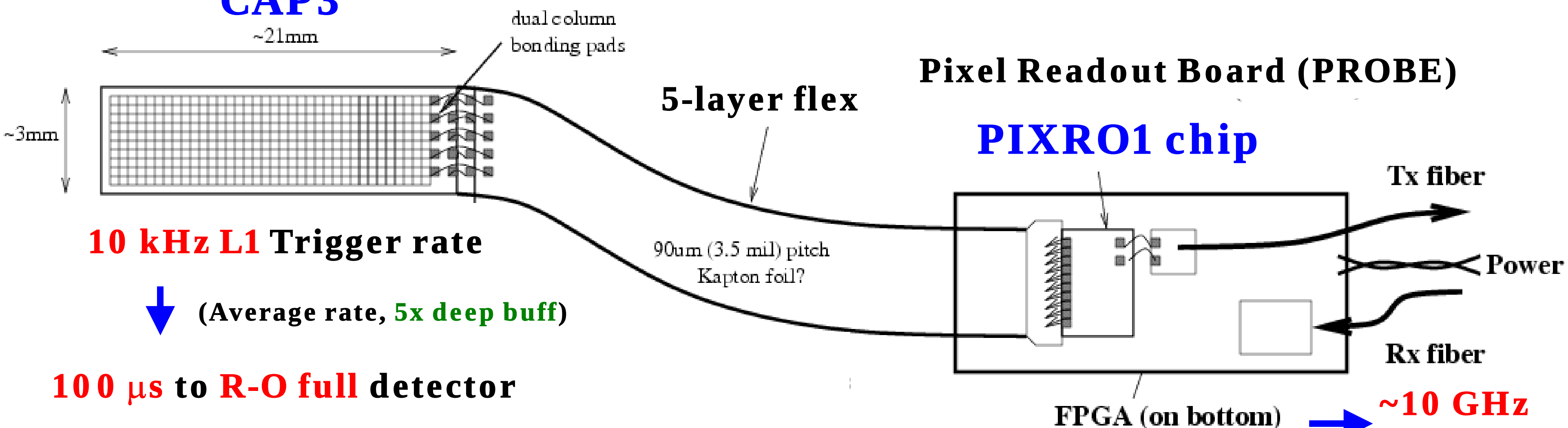
- Settling time on long bus lines too long (~1us, while <<100ns needed)



  – Large drive strength needed for fast, unbuffered signals (Select 0 "S0" ~ 750pF !!)

More Fundamental: data flow

CAP3: 10μs frame rate (experienced with CAP2)
Super-Belle: 10kHz L1 Trigger rate



10 kHz L1 Trigger rate

↓ (Average rate, 5x deep buff)

100 μs to R-O full detector

↓ (~1k column x 2samples)

100 ns / column

↓ (128 rows x2, 32 8:1 MUX)

2o ns bus settl., 10 ns/sample

→ **16 pairs of signals** (100 MHz signals) →

16 CDS

Differential receiver

↑ (high speed analog 16:1 MUX)

1.6 GSa/s analog (6 bits)

↑

(embedded sample) → **~10 GHz analog**

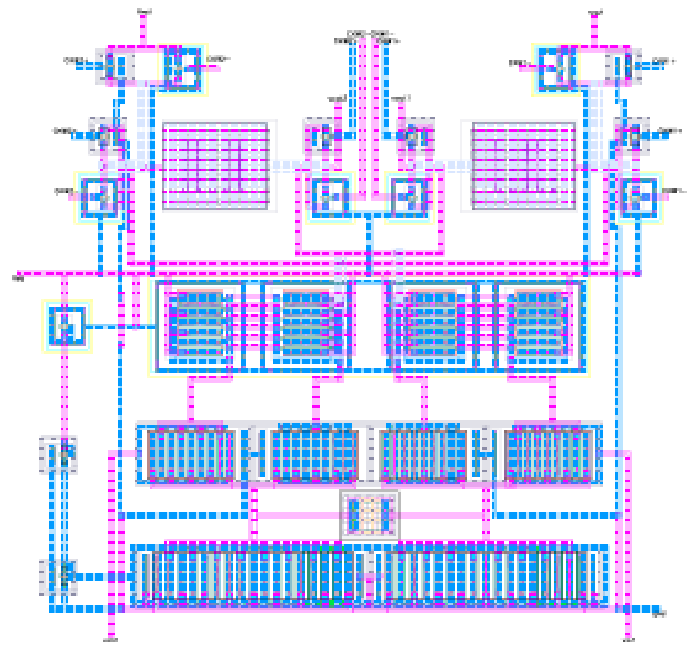
PIXRO1(1): Output Amplif.

Basic Concept

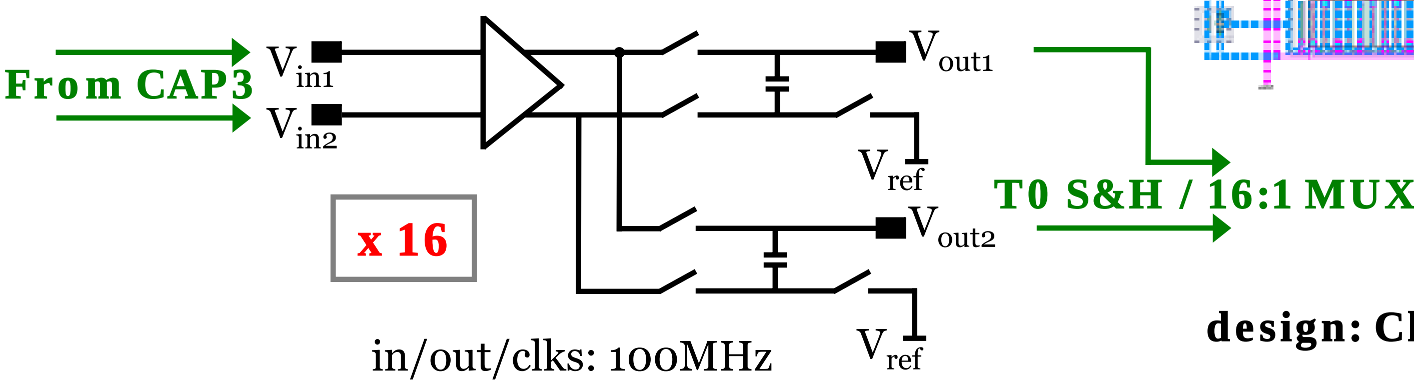
1 CAP ⟷ 1 PIXRO1

SiGe 0.5μm process from IBM

First version of PIXRO chip:
(relative) simplicity



Amplifier: Diff→Single Ended (fr2-fr1)



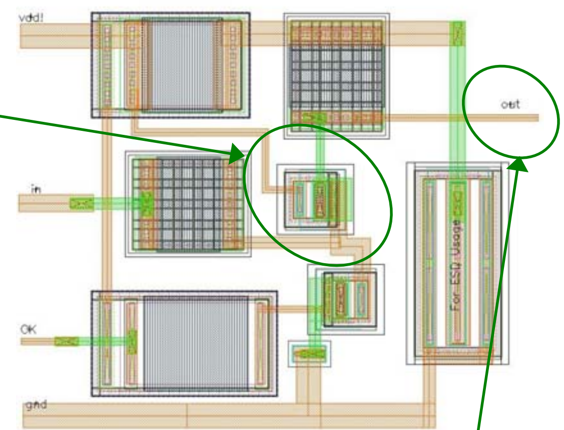
design: Chenyan Song (UH)

PIXRO1(2): S&H and 16:1 MUX

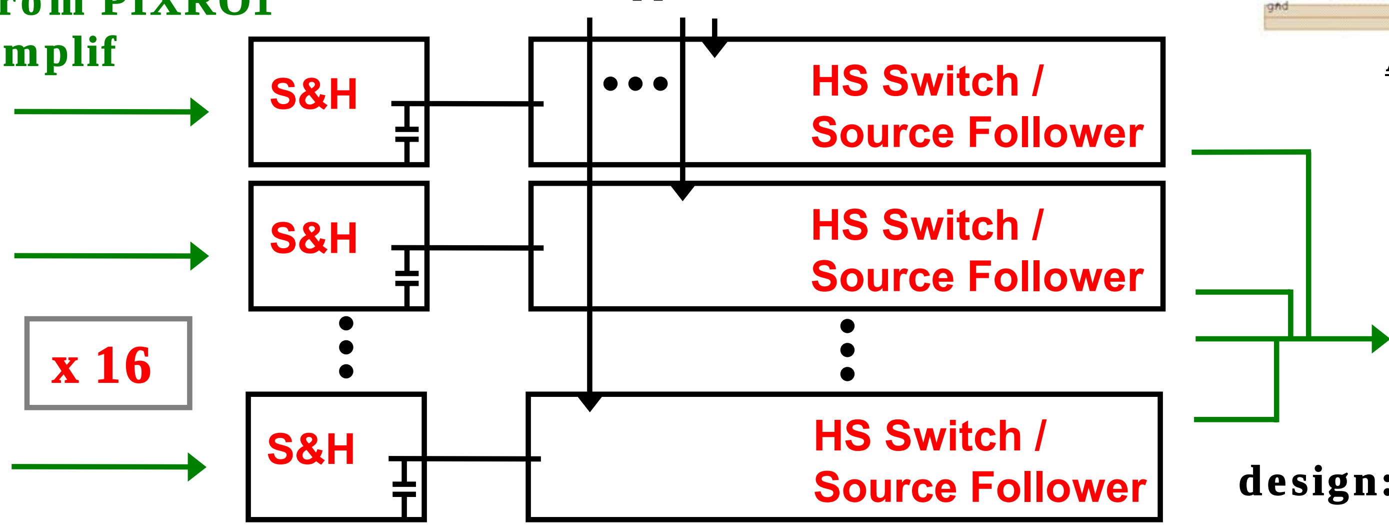
Basic Concept

SiGe 0.5µm process from IBM

NPN switches & SF for high speed



A HS Switch/SF



design: Qianyi Yang (UH)

Problems (III)

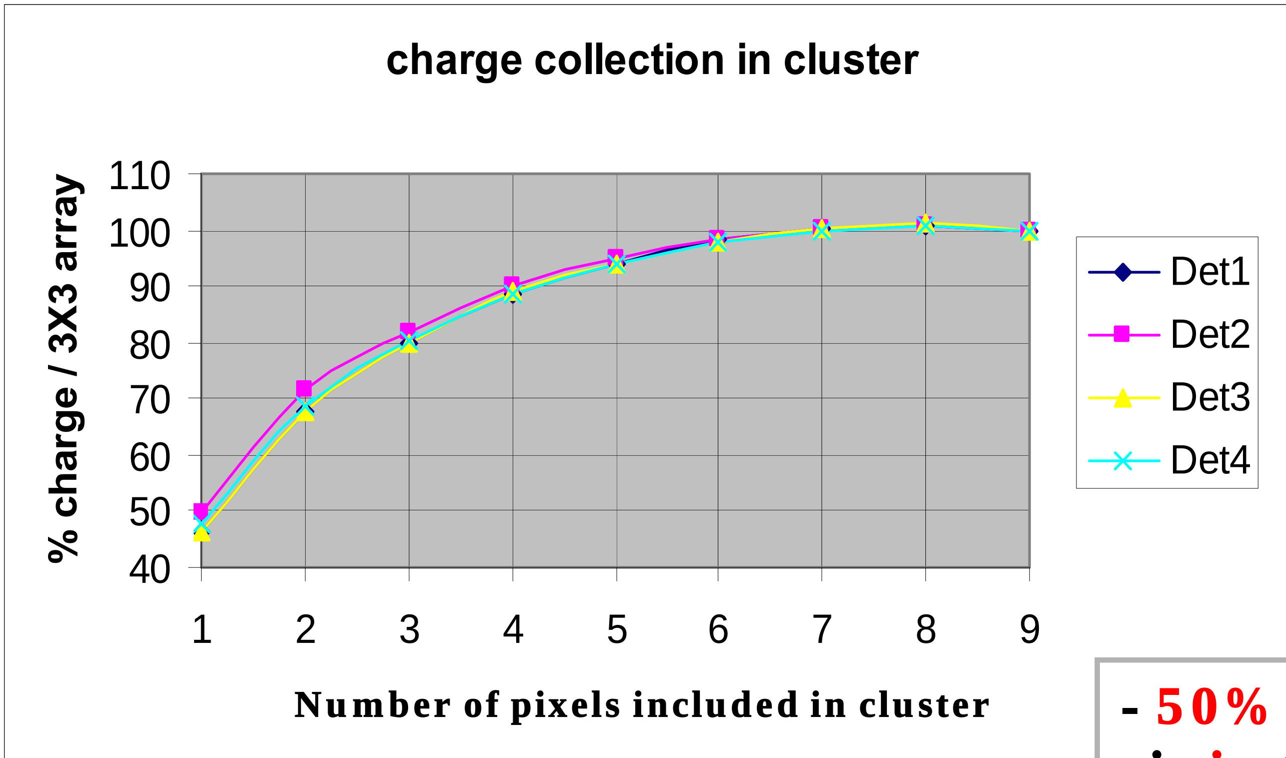
- In Belle Note # 772 Presented 4x readout schemes
- Pixel Readout #1 (PIXRO1)
  - Extensive design and simulation (3x Masters'/PhD EE students) indicated basic scheme could not be made to work in a process we can afford
    - IBM bi-CMOS (SiGe process) has NPN transistors > 60GHz f_tog HOWEVER, PNP is slow → not possible to push-pull
    - Useable operating range is very small; difficult to control offsets
  - High speed analog link good for RF, not discrete level signals
    - Settling time, cross-talk and DC drift problems
- TSMC 0.25um process (8um Epi) → AMS 0.35um OPTO process (thick epi)

Next Directions

- CAP4
  - Modify storage/output scheme
    - Time-encoded readout (no direct analog)
    - In-pixel CDS
  - Lessons learned in layout
    - Match North-South/East-West transistor orientation
    - Adjustable reset transistor VDD

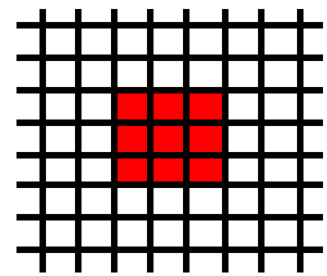
- CAP5
  - Radically different architecture: smaller pixels, binary readout
  - More in the spirit of original CAP concept – continuous readout (no trigger rate limitation)

Charge Spread in CAPS



(MPV of landau fit)

Hyp: charge entirely collected in 3X3 pixel array.

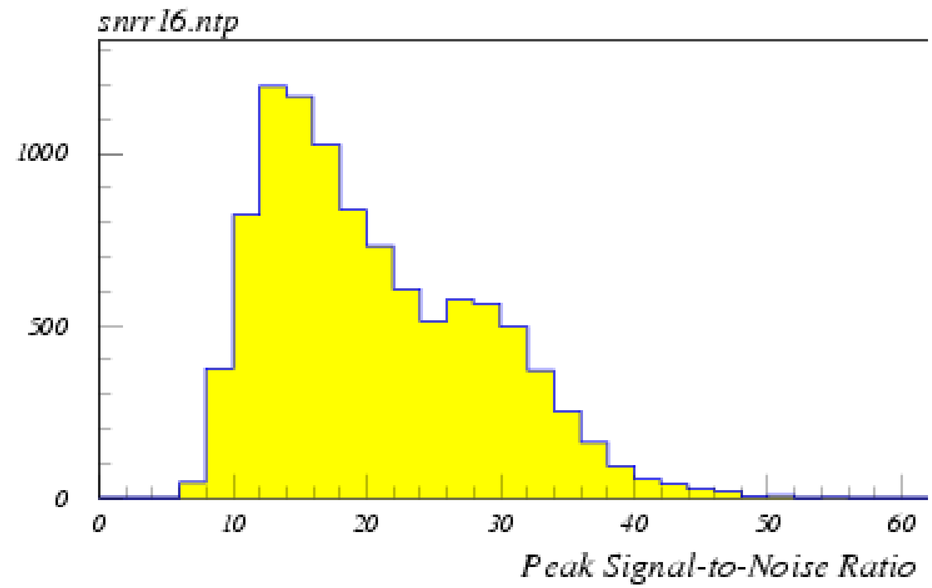


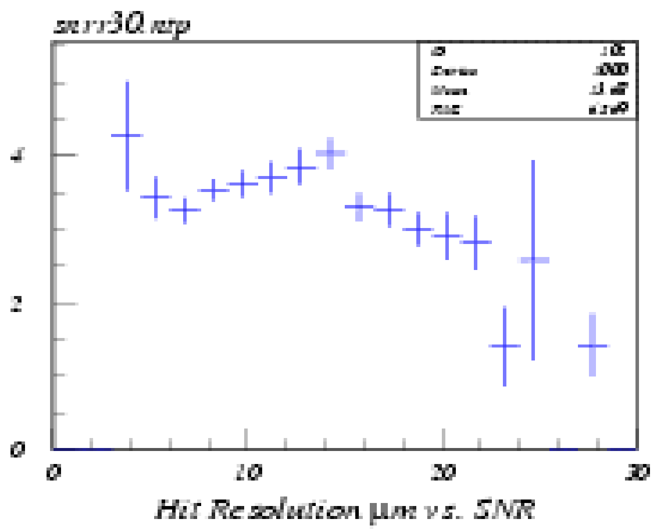
- 50% of the charge is in the peak pixel.
- 90% in the 4 largest.

Hit resolution vs. SNR MC

Toy MC:

1) Generate random impact parameter
2) Landau fluctuation of signal
3) Charge diffusion (thermal)
4) Add noise (16e-/30e- system)
5) CoG of hit calculation





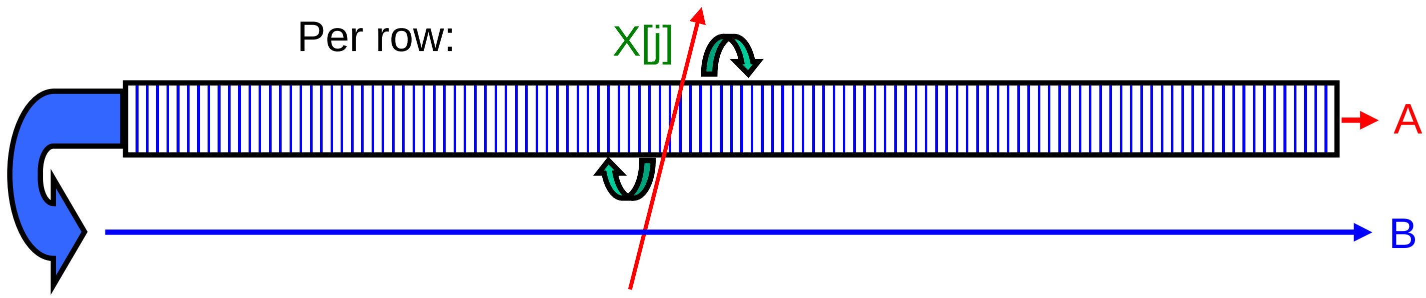
Good hit resolution even at low SNR

Note binary limit:
22.5µm/sqrt(12) ~6.5µm

CAP5

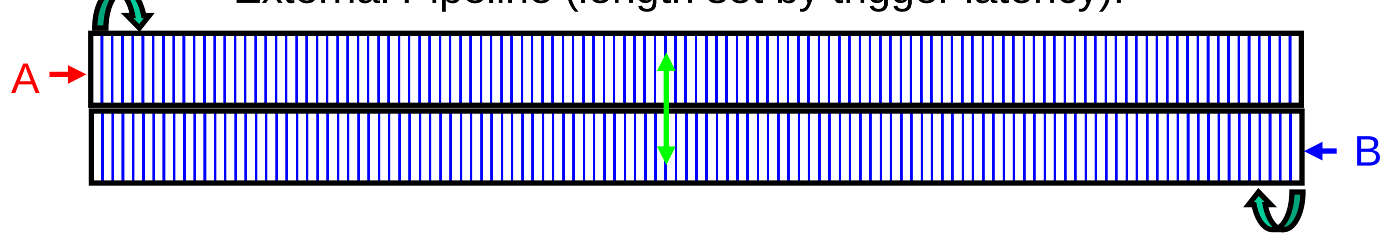
- Binary Readout (11.25um/SQRT(12) ~ 3.25um)
- 100ns sample steps – values shifted out left/right

Per row:



- Use temporal coincidence and match with trigger to reconstruct position and reject out of time hits

External Pipeline (length set by trigger latency):



At trigger latency time, A&B = 1 @ X[j]

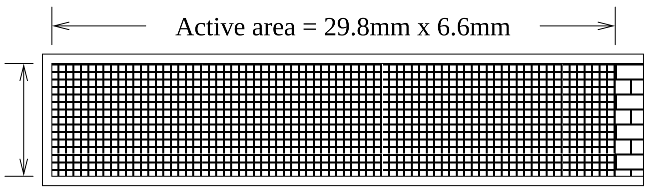
Occupancy Scaling – CAP5

- Work from following assumptions:
  - Super-B (conservative) **x50** background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm^2
  - CAP5 Pixel spatial reduction:
    - Pixel area = 11.25μm x 11.25μm = 126 μm^2
    - Reduction factor ~ 33,700
    - Low E γ, reduced cross-section (~3% active thickness)
  - Pixel temporal reduction:
    - 1.0μs SVD vs. 100ns
    - Reduction factor ~ 3 (consider 3 samples needed)
  - Grand total:
    - 10% * 50 * $33{,}700^{-1}$ * 3^{-1}
    - Can expect ~ 0.005% occupancy

Event size – CAP5

- Conservatively take 0.01% as Occupancy

R = 1cm case



~1.55M channels/detector

2 layers * 20 HL = 62M pixels

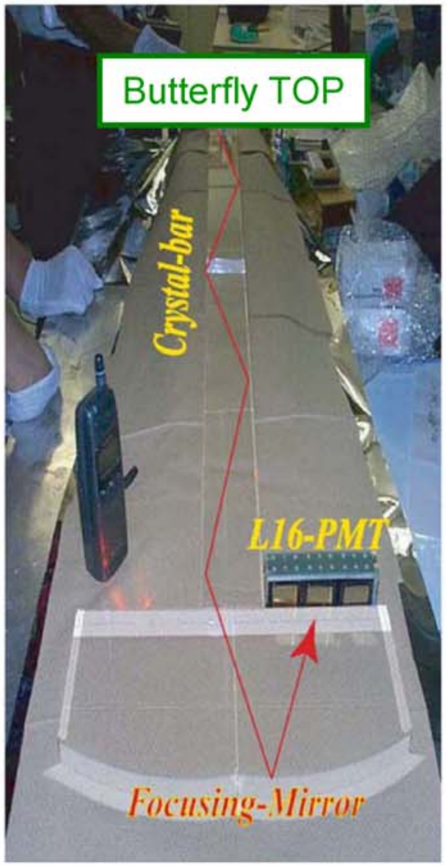
6.2k Pixels Hit/event

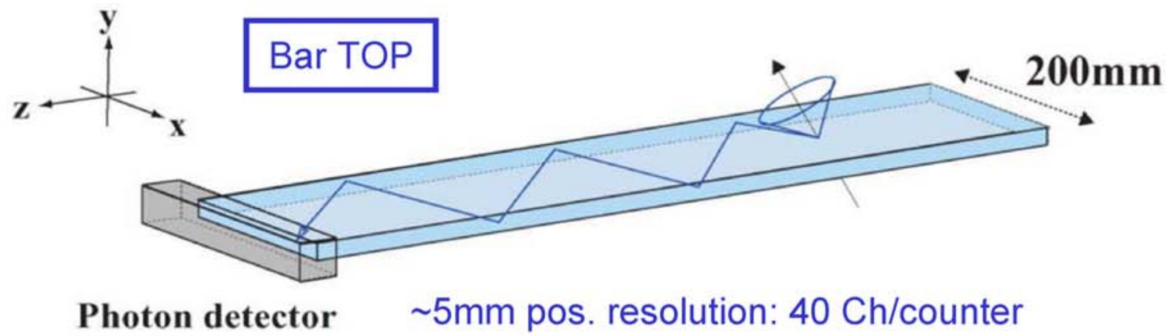
- 1 bit/pixel
- However, need ~26 bits of address info
- 4 Bytes/pixel → 24.8kB/event
- No need for track matching

CAP5 readout

- Output bits can be multiplexed onto LVDS lines
- Natural zero-suppression with trigger matching
  - No "long lines" to drive fast, yet fine time segmentation
  - No complex buffer matching, >>10kHz L1 possible
- Coincidencing pipeline implemented in a standard FPGA → slow LVDS or Multiplexed (many detectors) Fiber link to FINESSE/COPPER system

SuperB Barrel PID Upgrade





~5mm pos. resolution: 40 Ch/counter

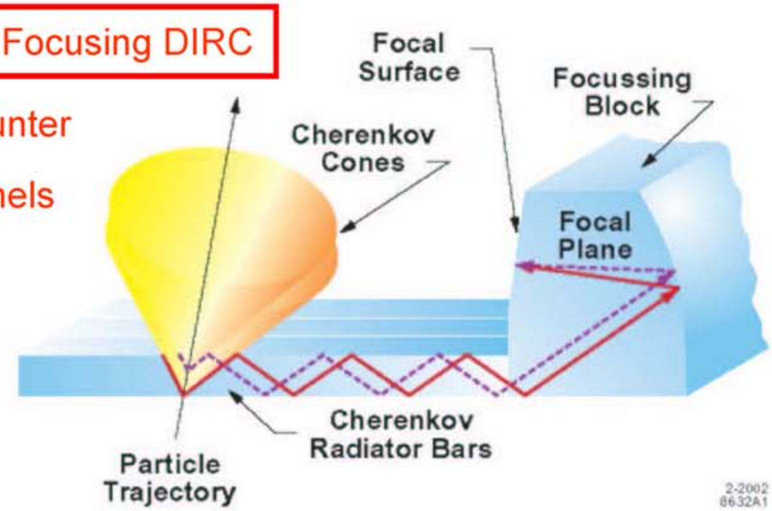
*200 counters = 1440 channels

Multi-hit (hidden cost) >1440 channels

Focusing DIRC

~few mm x few mm: few kCh/counter

*~100 counters: few 100k channels



~1mm pos. resolution: 200 Ch/counter

*180 counters = 36,000 channels

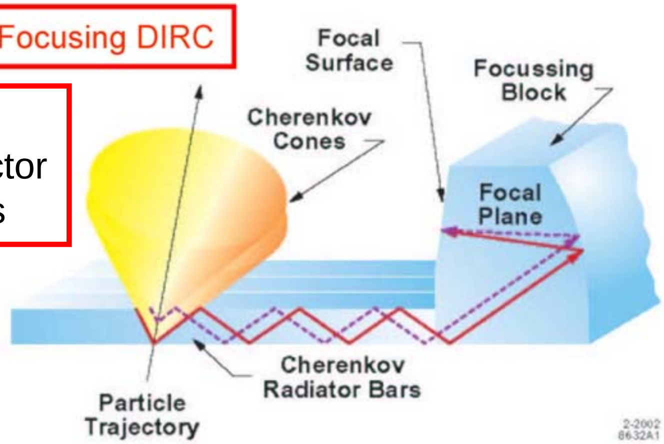
How to Read Out ?

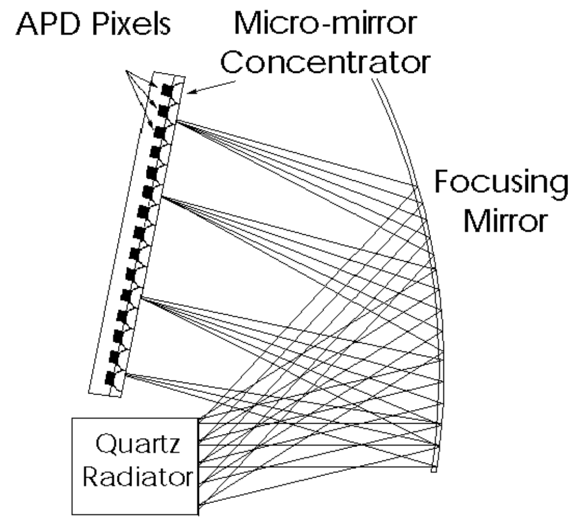
- 10's – 100's k channels
- Fine time (25ps?) resolution
  - TOF for pf-RICH, f-DIRC
- Pile up – high rate
- Highly integrated

e.g. f-DIRC Upgrade

Focusing DIRC

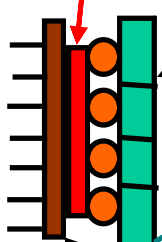
Many k Photodetector channels





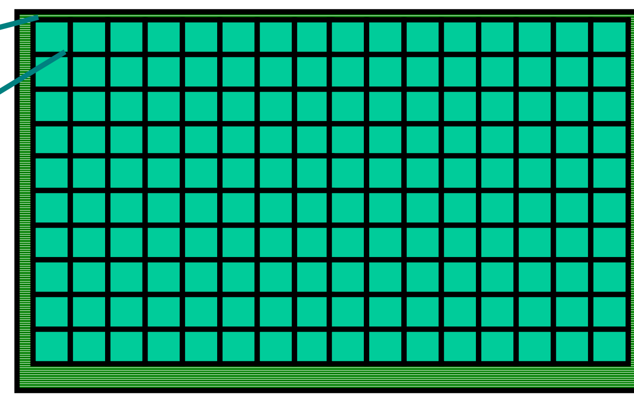
ASIC

Single Module: (side-view)



APDs

Carrier Socket



Tiled Array

Readout Board

PID Upgrade Readout

ASIC Concept 1: Continuous Hit logging

- Based on waveform sampling technology
- No high-power comparators (on detector)
- Almost no overdrive required (low power)
- 4x interleave buffering → deadtimeless
- Digitize immediately "high" threshold:

4GSa/s→1/SQRT(12) ~70ps
- Record "low" threshold simultaneously

→ improve to ~50ps (SQRT(2))?
- Also measure Time-Over-Threshold (Q)

→ provide pile-up rejection in 50ns window
- Pipeline on FINESSE or detector?

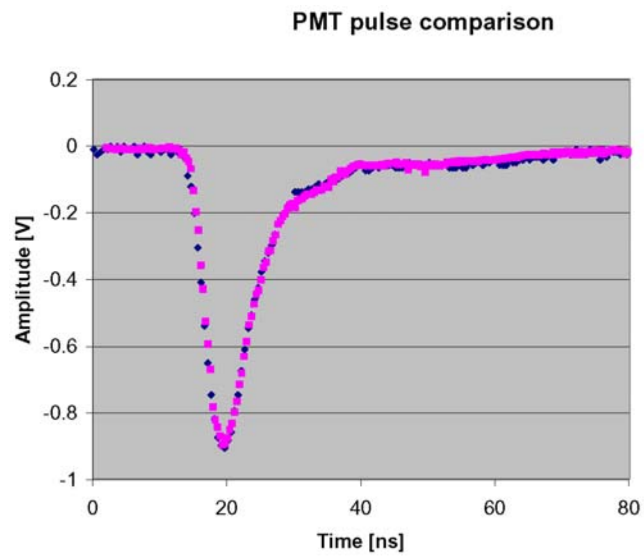
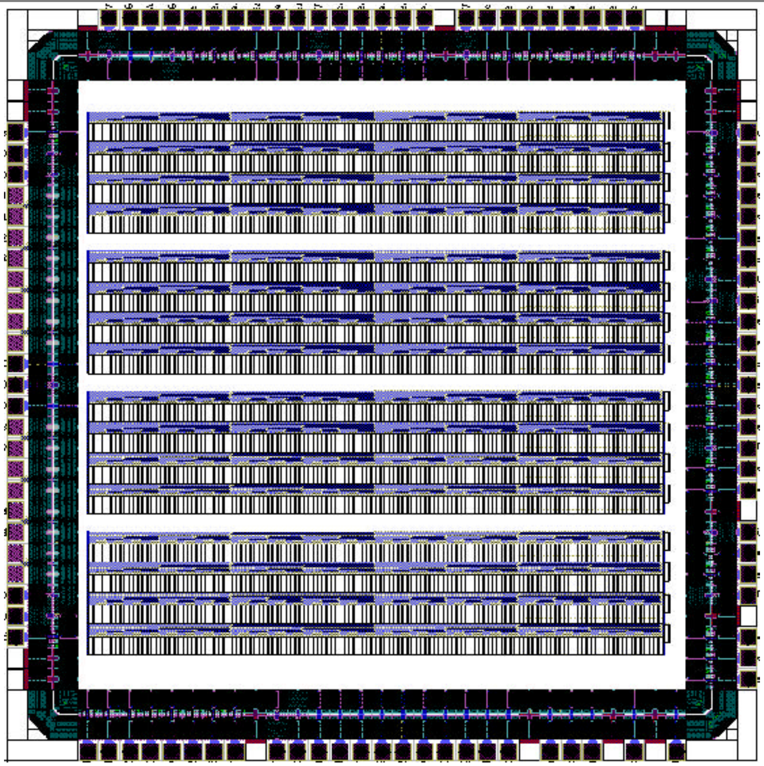
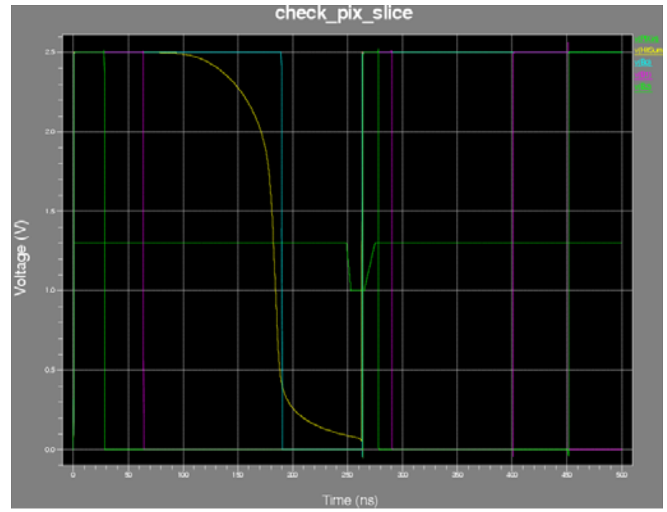


Photo-detector ReadOut (PRO1)

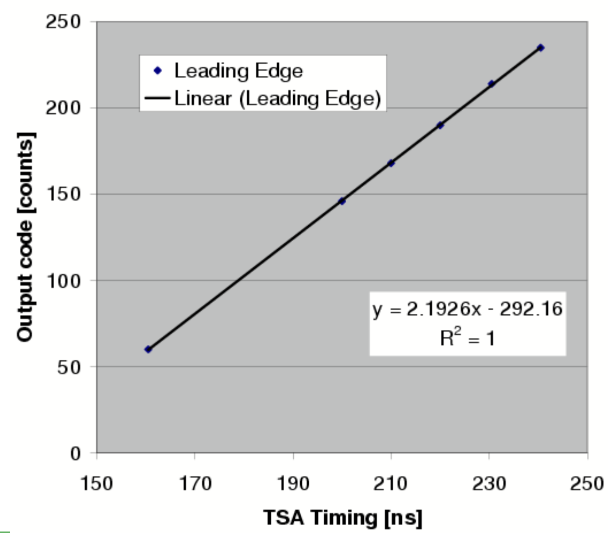


PRO1 Die floorplan: 4 (H)APD channels
4 x 256 samples
In a 2.5mm x 2.5mm die

PRO1 version submitted in February
TSMC 0.25um



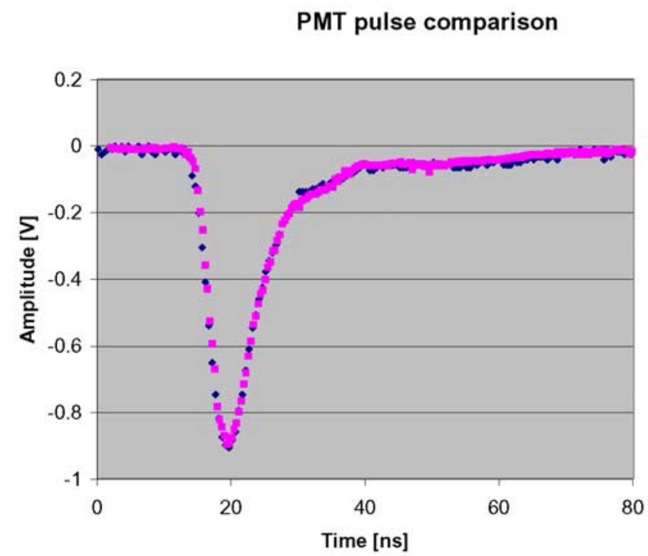
SPICE Simulation of PROMPT Response



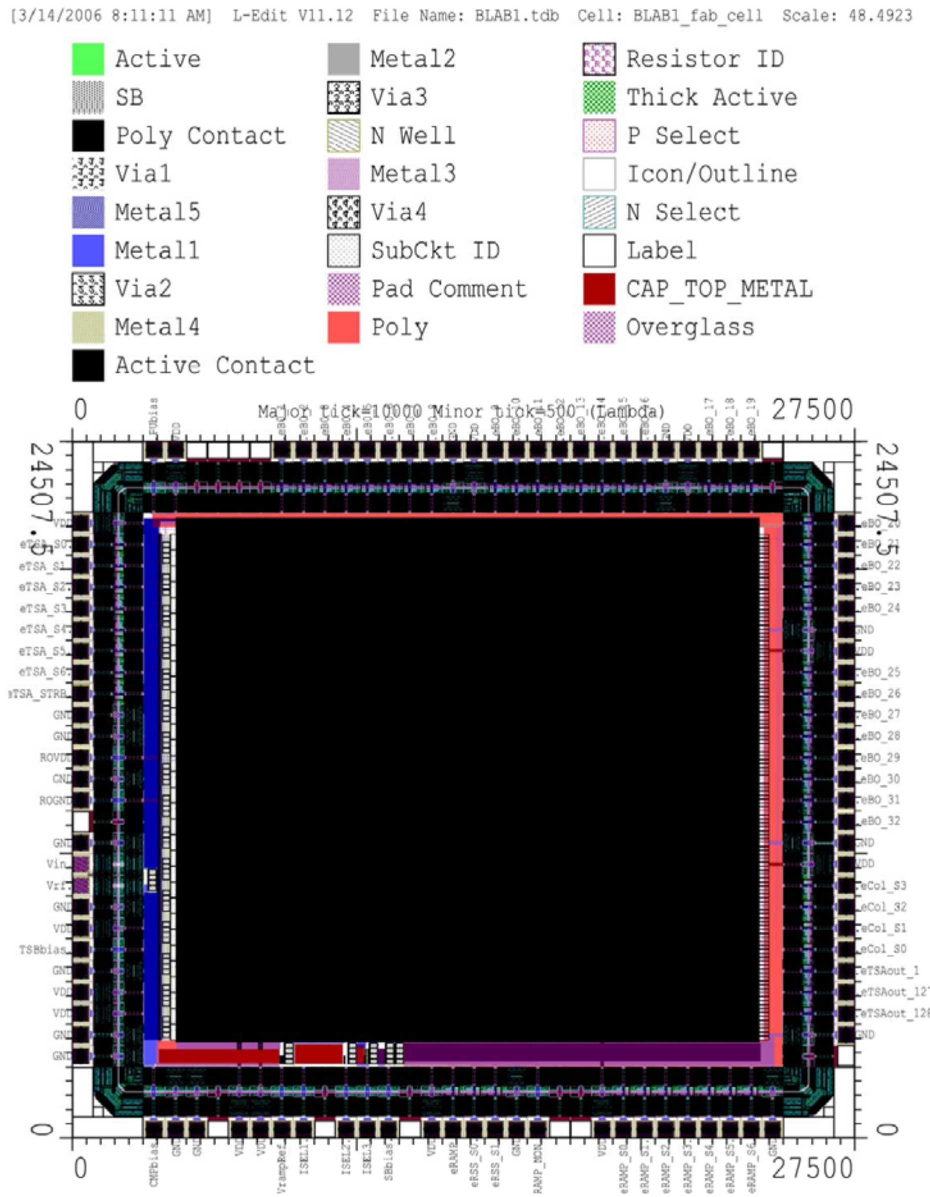
PID Upgrade Readout

ASIC Concept 2: Deep, fast analog pipeline

- Based on waveform sampling technology
- Take LAB3 architecture (260 deep) and extend to 65k samples
- Overkill for single p.e. device?
- High-speed parallel digitization/readout → extra depth to allow continuation of sampling while reading out (effectively pipelined)
- ADC precision adjustable
- Extract hits/zero suppression needed up-front



Buffered LABRADOR (BLAB1)



16μs storage at 4GSa/s

32 parallel Wilkinson outputs to companion FPGA

16-bit precision, oversampling possible (storage kTC limited)

ASIC submitted last Monday

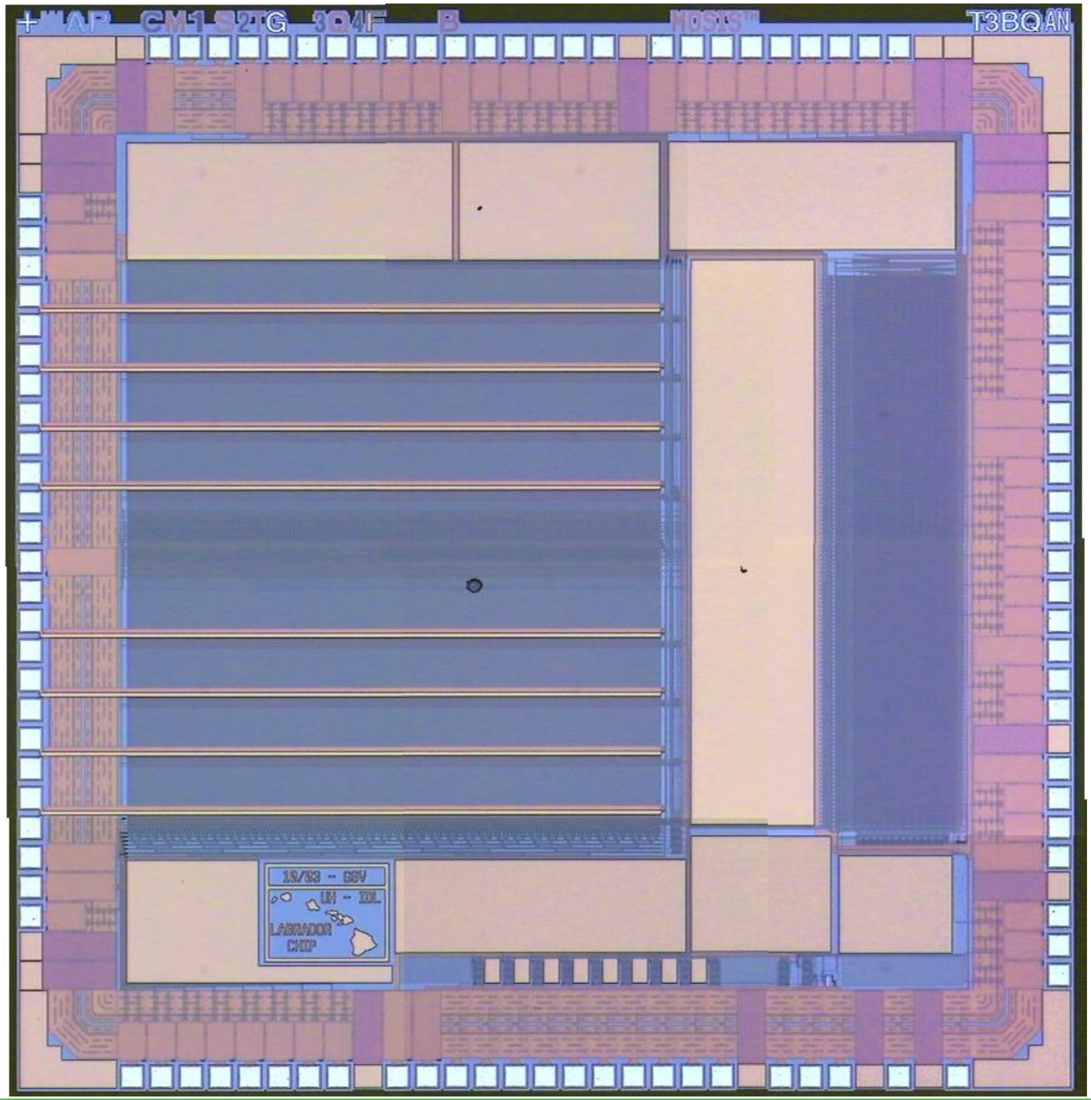
BLAB1 Die floorplan: 1 (H)APD channel
In a 3.3mm x 2.9mm die
TSMC 0.25um

Summary

- CAP Architectural Development
  - Learning what is possible in MAPS
  - Next test ASIC submission (CAP4/5) April 17th
  - Possibility to reduce data flow and use commercial FPGA for readout stream

- Precision timing PID Readout
  - New ASIC developments (new chips in summer)
    - High-density, low-power, fine time resolution
  - Readout/incorporation into FINESSE/COPPER system straightforward

Back-up slides

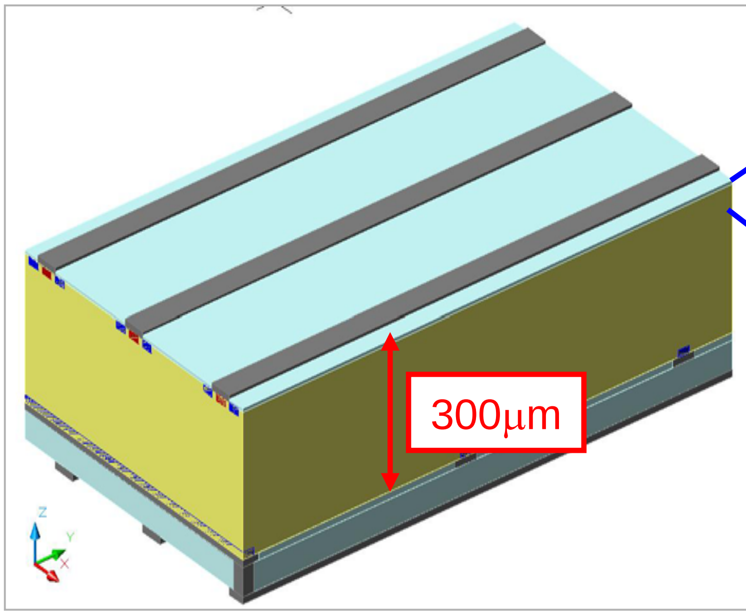


Why bother with a Pixel Detector?

- Occupancy
  - Current SVD simply won't work @ higher Luminosity (instigating progress)
- Improved vertexing (already a Super-B Factory)
  - e.g. better continuum suppression → improve background systematics limited analyses
- Be competetive (aggressive)
  - To remain viable, continue to look for ways to **exploit** B-factory benefits

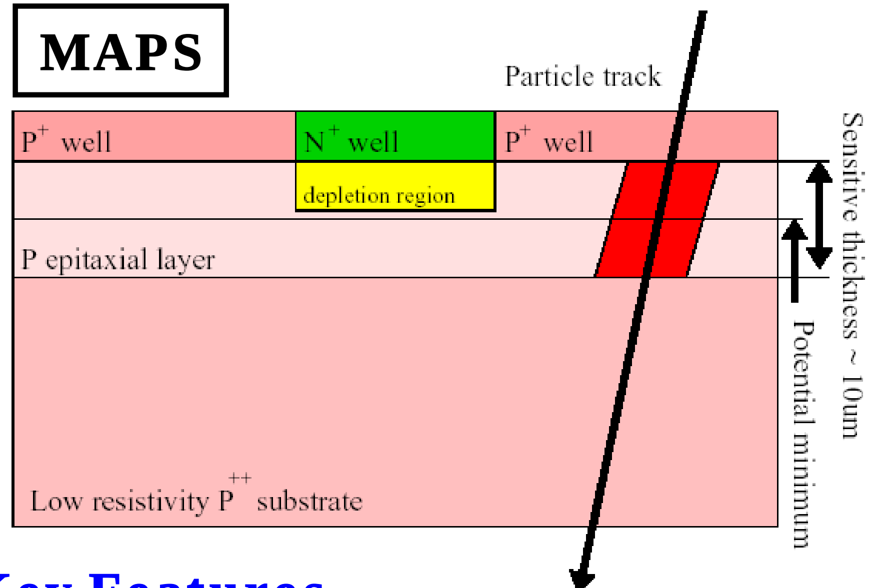
Candidate: Monolithic Active Pixel Sensor

Current DSSD



Because of large Capacitance, need Thick DSSDs -- APS can be VERY Thin

MAPS



Key Features

- Thermal charge collection (no HV)
- Thin - reduced multiple-scattering, γ conversion, background γ target
- NO bump bonding – fine pitch possible (8000x geometrical reduction)
- Standard CMOS process - "System on Chip" possible

Hits! alignment proof