Recent Progress in the Development of a Monolithic Active Pixel Detector for a B-Factory

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Abstract

Monolithic Active Pixel Sensors (MAPS) may become the building blocks of vertex detectors at future high luminosity e^+e^- colliders. Requiring an active layer only a few tens of microns thick, MAPS can be thinned to $\sim 50\,\mu$m, which reduces the multiple scattering of primary particles. Deep sub-micron CMOS processes allow for small pixel size, needed for adequate single point resolution and low occupancy at a Super B factory. Major concerns with MAPS are readout speed and signal stability for large pixel arrays. Laser bench test results of a full size prototype (CAP3) with 118,784 readout pixels and a 5-deep correlated double sampling pipeline are presented. Lessons learned are applied to a design iteration and investigation of two new digital readout sensor designs, all included in the CAP4 prototype chip.

Key words: B factory, Vertex detector, Monolithic active pixel sensor, CMOS, Radiation hard
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1 Introduction

Monolithic Active Pixel Sensor (MAPS) technology has been developed for use in the vertex detector (SVD) of a collider experiment for over ten years [1]. At first glance, MAPS seem to be one of the best suited technologies for use in an SVD at high luminosity e^+e^- colliders such as the future International Linear Collider (ILC) or an upgraded version of B factory [2,3]. Using small pixels, MAPS devices can give excellent single point resolution and very low occupancy. Moreover, as the active area of the sensor occupies only a small fraction of the usual 300 μm silicon die thickness, it can be thinned, which reduces multiple scattering in the low momentum track environment of these colliders. Strip detectors used presently in the Belle vertex detector [4,5] are in contrast relatively thick, and at high luminosity the problems of high occupancy and hit assignment ghosting will occur. The hybrid pixel detectors developed for the LHC are much thicker than MAPS [6,7]. Strip and hybrid pixel technologies are therefore not optimal for an e^+e^- collider with a luminosity of several $10^{35}/\mathrm{cm}^2/\mathrm{s}$ and medium-energy particles.
However, before MAPS can be accepted as potential precision tracking devices, sufficiently high readout speed, stability of device characteristics after thinning, tolerance to radiation, and the scaling up of the initial small-size prototypes to real size detectors has to be demonstrated. Two early prototypes, the Continuous Acquisition Pixel (CAP) 1 and 2 have been developed [8] in the context of the Super-Belle upgrade. With these unthinned 6,336-pixel devices it was possible to establish the basic functionality of CAP for high precision tracking. The third prototype (CAP3) is a 118,784-pixel array, and is large enough to serve as a building block for a vertex detector. During its testing, several design flaws became evident, such as its limited dynamic range, poor choice of the reset transistor control, long settling time on highly capacitive (long) bus lines ($\gg 100$ ns required) and large drive strength needed for fast, unbuffered signals. A new, faster, time encoded analog readout scheme to fix the above problems is a part of the CAP4 prototype, as well as two new digital readout schemes. These digital schemes employ smaller pixel sizes and binary continuous readout with no trigger rate limitation.

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2 The CAP3 prototype

The base pixel structure of any of the CAP1-CAP3 prototypes is simple: a standard MAPS cell architecture, consisting of a "sense" transistor (for transconductance measurement of the charge collected in the sensor), a "reset" transistor (to restore the collection potential to the sense transistor) and selection mechanism (to select a pixel for readout). CAP3 is the first prototype large enough in size to be able to become a building block of a pixel vertex detector. A die photograph and the schematics and layout of a pixel base cell of are shown in Figure 1.

CAP3 consists of 928 columns × 128 rows, and is implemented in the 0.25 μm

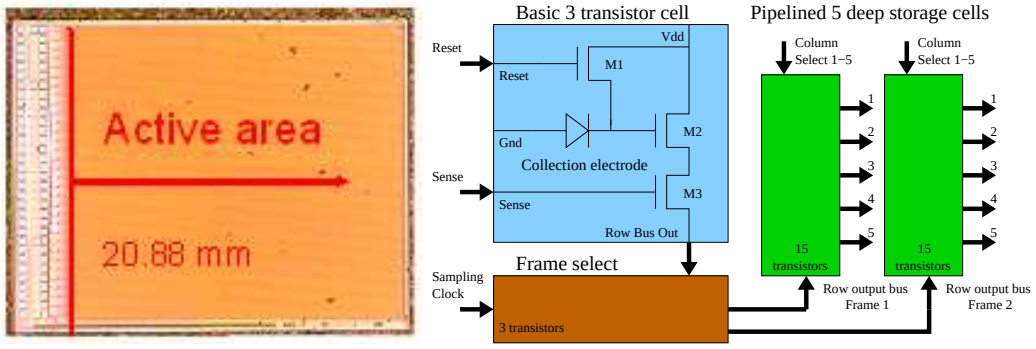

Fig. 1. Photograph of the CAP3 prototype with 928 × 128 pixels (left), each 22.5 μm × 22.5 μm in size. The total sensor size, 20.88 mm × 3 mm, has been rescaled for the sake of display convenience. A schematic of the pixel cell (right) shows 5 sets of pipelined internal storage cells per pixel, which require 36 transistors, thus CAP3 sensor contains in total more than 4.3M transistors.

technology from TSMC [1] . The base pixel size of 22.5 μm by 22.5 μm was chosen to minimize the number of readout pixels while still obtaining sufficient single point resolution and low occupancy in a high luminosity environment. Due to the small feature size we were able to fit into each pixel a 5-deep correlated double sampling (CDS) pipeline, leading to a differential readout. To reduce power dissipation, current flow in the cell (Fig.1) can be switched off when not sampling, and a system of pre-sample and post-sample switches is provided to select the 5-deep storage buffer. Data are then read out differentially, each output going to a bus and to the chip output. There a selection of a specific differential pair for each row is made and the 128 double samples are multiplexed by 8 onto 16 parallel analog double sample output streams, which are first amplified and then sent out of the chip through a double-row of bonding pads.

The CAP3 readout follows the two-card scheme developed for previous CAP1-2 prototypes [8], with the necessary modifications of the front-end (FE) board so that it can accommodate the new detector (Fig. 2). The FE board includes

[1] Taiwan Semiconductor Manufacturing Company Ltd., Taiwan.

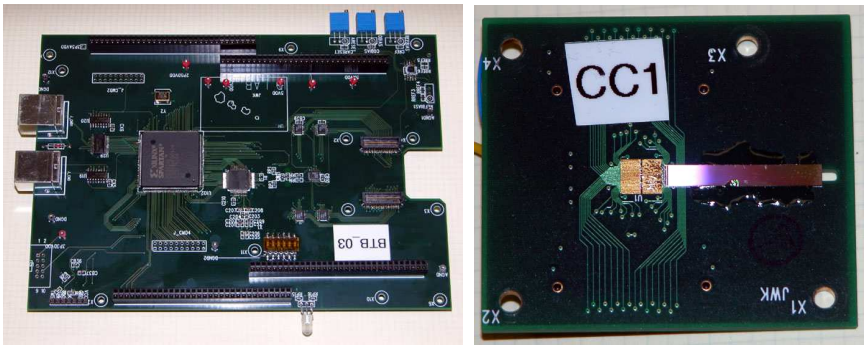

Fig. 2. Front-end (FE) board with the ADC converter, analog support electronics and the connectors (left), and CAP3 prototype bonded to a separate board for use with the FE board (right).

a 16-bit analog-to-digital converter (ADC) and the analog support electronics. To have maximal flexibility in the testing of the sensors, i.e. easy interchange of CAP3 prototypes and decoupling of FE board encountered features from the behavior of a specific sensor, CAP3 itself is wire-bonded to a separate carrier board, which is pluggable into the FE board. Four 60-pin connectors on the FE board allow for mechanically stable stacking of boards and bring the power supply voltages from a separate power board at the bottom of the stack. Each FE board is connected to a compact PCI back-end (BE) board via two standard CAT5 Ethernet cables: one transferring the control signals and the other transferring data at approximately 400 Mb/s. Four FE boards can be read out into a single BE board to simplify event synchronization when operating with an array of up to four detectors. The data from the BE board is read out by an embedded CPU running Linux OS via a PCI interface.

2.1 CAP3 test results

The first measurement with CAP3 was the noise measurement (Fig. 3). It was found that the addition of a storage cell did not lead to a large increase of the noise ($\sim 25\,e^-$) compared with the results for the CAP1 ($\sim 16\,e^-$) and was better than CAP2 ($\sim 35\,e^-$). As CDS is done with sample pairs in both CAP2 and CAP3, the improved noise is partially attributable to the reduction in fixed pattern noise due to the differential readout of the two sample pairs, coincident in time. This result confirmed that the differential readout scheme successfully reduced the system noise pick-up.

Tests of the detector response and performance of the CDS pipelined readout were made using a laser test bench. As the front of the CAP3 is covered with 5 metal layers to accommodate the connections between the 3-transistor cells and storage cells, which reflect light, the sensors had to be back-plane illuminated with an IR laser (960 nm) which can penetrate through $250\,\mu$m of the Si bulk. The laser beam was pulsed, with a pulse length of a few μs

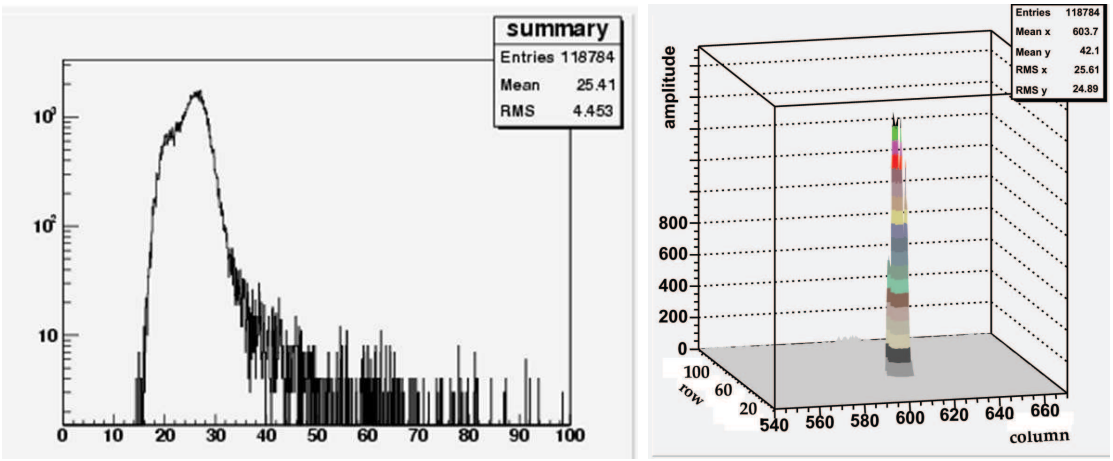

Fig. 3. Left: Noise distribution for the 118,784 pixels of a CAP3 sensor. The mean noise was around $25\,e^-$. Right: 960 nm laser spot as seen by backplane-illuminated CAP3 detector.

and focused to an area with a diameter of about 10 pixels ($\sim 200\,\mu$m). A surface scan of the sensor was performed using a computerized X-Y stage. An example of the laser beam profile can be seen in Fig. 3, right. In different measurements the data was read out from all five storage buffers, one pair per event cyclically, to confirm the functionality of the internal storage pipeline. With the scans we discovered that 16 groups of rows connected to different readout multiplexers behave differently in terms of noise, and a systematic shift in transfer curve response column-wise was also found, so that a gain correction has to be performed.

Electronics tests, however, showed that CAP3 design suffers from several flaws. These are limited dynamic range across the entire chip for a common set of bias parameters, poor choice of reset transistor control for the basic three transistor pixel cell and excessively long settling times on the highly capacitive bus lines running the entire length (2 cm) of the sensor. As a result, in the next design, the readout has been modified to include a Wilkinson type ADC on the chip, which should greatly reduce the settling time on the long bus lines. The reset transistor circuit has also been redesigned and a buffer amplifier has been added. Regarding the readout speed, it has so far been limited by the performance of the support electronics, and will for the next prototype of the sensor be upgraded to evaluate possible DAQ degradation at higher acquisition rates. Radiation hardness of the sensor, especially the evolution of its leakage current as a function of irradiation, will also be further studied with the next prototype, CAP4.

3 The CAP4 prototype

In 2006 a new prototype (CAP4) was made in the AMS 0.35 μm Opto process [2], with a thicker epitaxial layer than the previous CAP1-3 chips [9]. The CAP4 chip contains three separate sensors, following two conceptually different designs, one analog and two different "binary output" ones (Fig. 4). The first design aims to further develop the analog CAP architecture already implemented in CAP1-3 prototypes, and the second one to test basic functionality of a new digital readout concept, which is, in contrast to the analog one, trigger rate independent. Read-out electronics and the test stage are in preparation. A beam test experiment is planned at the new 3.5 GeV electron testbeam line at the KEK FUJI hall in the fall of 2007.
The analog part of CAP4 is made of 132 columns $\times$ 10 rows of pixels, and the size of each pixel unit cell (PUC) is 22 μm by 25 μm. The pixels are still the previously used 3-transistor cells with a redesigned reset transistor control for better tuning of the readout chain. A new bus architecture based on a "tree-readout" has been used inside each row to reduce the capacitive loads of the long output bus lines that run across the columns, and, thus, speed up the data output capability. Streaming of the data out of the chip is facilitated by encoding the analog signal levels into time intervals – the basic Wilkinson type ADC encoding – where the high-speed clocking is performed outside the CAP4. This allows the use of stronger, digital output buffers and improves the output drive strength. With the analog CAP4 we hope to obtain better parameter uniformity throughout the pixel array and higher data output speeds compared to the older CAP prototypes.

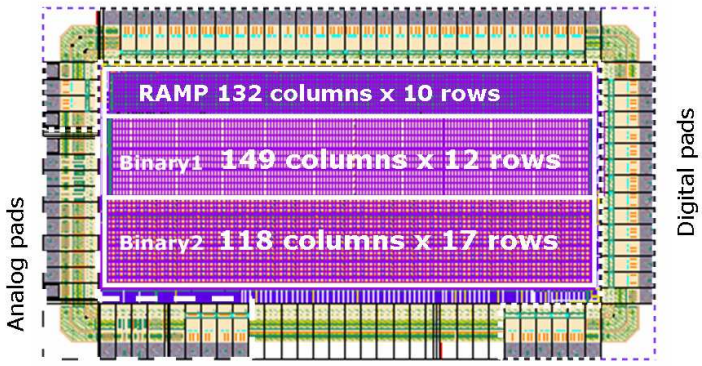

Fig. 4. Schematic view of a CAP4 prototype, containing an improved analog design MAPS (denoted as RAMP) and two new digital designs with continuous readout (denoted as Binary1 and Binary2).

The two digital readout sensors included in the CAP4 chip are arrays of 149 $\times$ 12 pixels (Binary1) and 118 $\times$ 17 pixels (Binary2), following the same

[2] MOSIS IC Fabrication Service, USC Information Sciences Institute, USA.

conceptual design. Binary2 is designed in PMOS, whereas in Binary1 NMOS has been used where possible to reduce the amount of PMOS; the use of PMOS in MAPS should be avoided because of parasitic charge collection at the extra N-well. By examining both we will try to establish the functionality of a new readout concept, where the data is being "continuously" streamed out of the sensor without any trigger rate limitation. The pixel unit cell (PUC) is based on the same 3-transistor structure as in the analog CAP4, however, the analog signal from the charge collected at the electrode of each PUC in one clock interval (100 ns) is fed directly into a comparator, which gives digital information. When the charge is above a certain threshold in a certain PUC, the local digital buffer is set to 1, and in every clock interval this digital bit of information is shifted to both left and right adjacent pixels in the same row as the hit PUC. After every shift an OR of the transferred bit and the bit of data from a potential hit occurring in the next clock interval in these two adjacent PUCs is performed, and so on. The hit information is transfered from PUC to PUC in the row in both directions, until it reaches either end of the row. On the readout side, output drivers broadcast the data out of the chip, and on the side opposite to the readout the same type of drivers send it in one clock interval across the complete array to the output. With this read-out scheme we should benefit from working with digital signals - driving the bus across the chip will no longer be a problem and noise pickup should be reduced. The requirements for speed should also be much easier to fulfill. The quantity of data broadcasted from the sensor would also be considerably reduced with respect to the analog readout schemes due to the intrinsic data sparsification. As the digital PUC size can in principle be reduced to about a half of the analog CAP PUC size (only one internal digital buffer is used instead of a large analog pipeline), the digital design would still provide excellent intrinsic resolution of around $3.25\,\mu$m.

4 Conclusions

With CAP3 sensors we have demonstrated that full SVD upgrade size detectors with pipelined storage cells for each pixel can be successfully manufactured and operated. The noise level was found to be $25\,e^-$, less than $35\,e^-$ for the older reduced size pipelined prototype CAP2, due to a new differential readout. An attempt to fix other flaws that were found (long settling times of the bus lines, reset transistor control and limited dynamic range) was made in the new CAP4 analog design. The CAP4 chip also includes two new digital readout sensor designs in an effort to increase readout speed, reduce noise and internally sparsify the data.

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