

Belle Monolithic Thin Pixel Upgrade

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Super B-Factory Workshop
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Univ. of Hawaii



Motivation

- Upgrade Advocacy (March 1997 Varner & Sahu^(a))
 - Simplistic evaluation of the raw contributions to vertexing
 - Argued for improvement
- Now update with valuable experience of excellent machines
 - Occupancy
 - * Current robustness is marginal. At 20x background, even with segmentation (“striplet”) and shorter shaping/pipelined readout – a concern
 - Improvement
 - Have been discussing in context of a x2 improvement
 - One of the few areas in which the detector can be improved to exploit Super B statistics

^(a) ”Pixel Detectors in a B-Factory Environment and thoughts on use in BELLE”,
Proceedings of the Second Workshop on Backgrounds at the Machine Detector Interface,
Gary S. Varner and Saroj K. Sahu, World Scientific, p. 162 March 1997.



Momentum Toward APS upgrade

- There has been much Active Pixel Sensor progress recently:
 - LEPSI/TESLA(MIMOSA) & LBNL/STAR prototypes
 - Hawaii has been evaluating STAR prototype
 - RAL (APV25) also getting into the act
 - Hawaii has made 2 prototypes (CAP1,CAP2) for B-factory
 - Will explain more about today
 - Beam test of Belle pixel proto sometime in 2004
 - There has been R&D into using hybrid pixels
 - Due to limited time won't cover
 - Simulation results show limited benefit – if too thick
 - In the spirit of “adiabatic” improvements, we may not have to wait for a “Super B shutdown”, can replace SVD inner layer with pixels – schedule dependent, we have experience
 - Quite low cost, most hard work done by industry

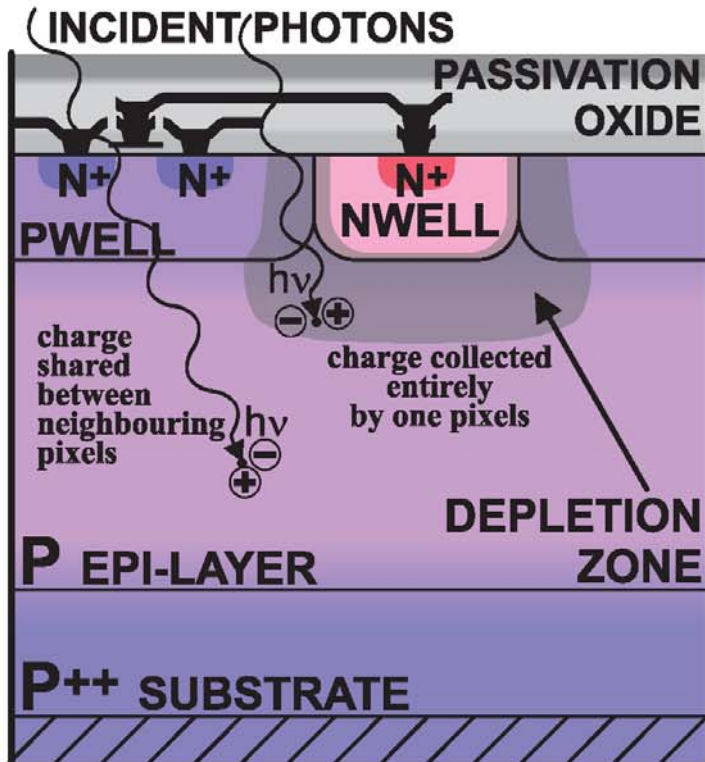


A Truly Attractive Proposition

CMOS Monolithic Active Pixel Sensors (MAPS) principle

“From digital cameras to particle tracking device”

W. Dulinski [LEPSI]



-The active volume (epi-layer, $\sim 10 \mu\text{m}$ thick) is underneath the readout electronics, providing 100% fill factor

-The charge generated by ionization is collected by the n-well/p-epi diode

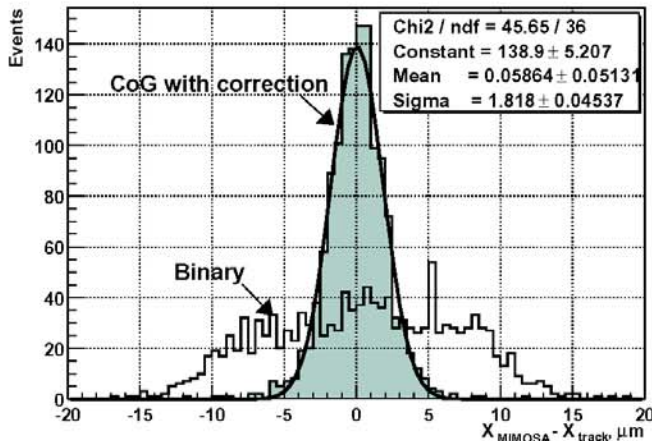
-Charge collection is achieved by the thermal diffusion

The device can be fabricated using a **standard, cost effective and easily available twin-tub CMOS process on epi substrate. No post-processing (e.g. bump-bonding)!**

System-on a chip approach possible

Promising Results

CMOS MAPS particle tracking performance (20 μm pitch)



ENC ~10 electrons: S/N > 30
Efficiency (5 σ seed cut): $\epsilon_{\text{MIP}} > 99\%$
Spatial resolution: $\sigma = 1.4 \mu\text{m}$

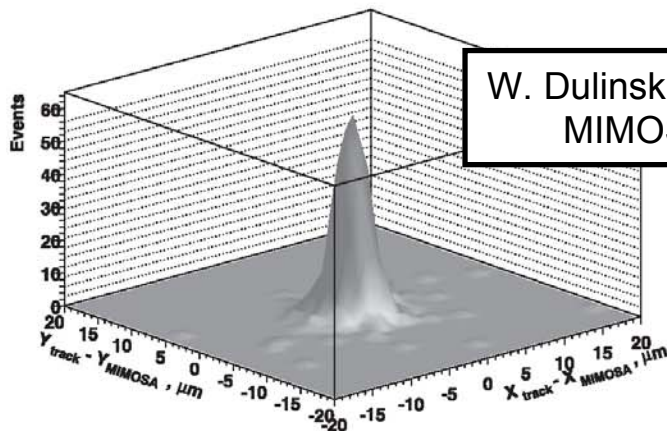
Demonstrated on several devices in various submicron CMOS processes:

AMS 0.6 μm , 14 μm epi
Alcatel 0.35 μm , 4 μm api
AMS 0.35 μm , no(!) epi

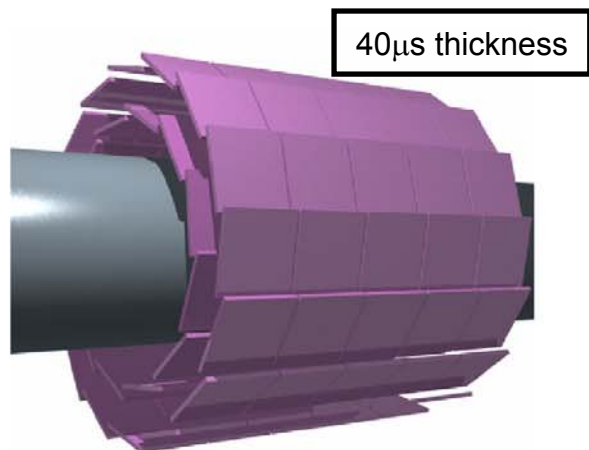
...

TSMC 0.25 μm , 8 μm epi
(LBL team)

+UH,
RAL



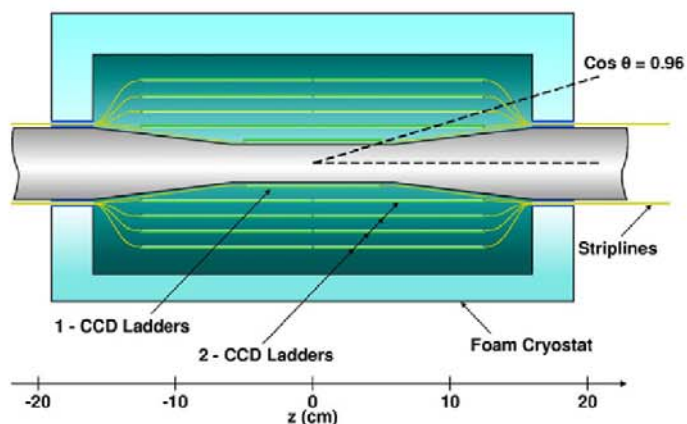
Other Experiments Considering



STAR μ vertex detector

1. First upgrade (x4 present luminosity, 2006):
10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008):
2 – 5 ms readout (integration) time

Super-Belle: 10 μ s ?



TESLA Vertex Detector*

1. Outer layers readout time: 100 -200 μ s
2. Innermost layer readout time: 25 -50 μ s

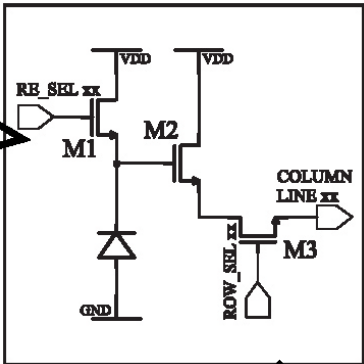
*NLC/JLC: $t \sim 10$ ms

Continuous Acquisition Pixel

- Conceptually Simple

- Analog reset, sample & then sample continuously
- Row-wise analog shift out as fast as possible:

- Consider $22.5\mu\text{m}$ pitch output w/ 4:1 AMUX
- 100MSa/s output (e.g. 8-bit ADC on output)
- $10\mu\text{s}$ for 1k columns (# row independent)
- Possibility of passing signals through to allow joining to form ladders

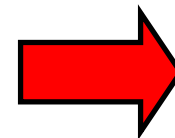


Standard APS pixel



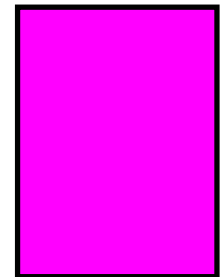
Pixel Array: Column select – ganged row read

High-speed



analog

ADC



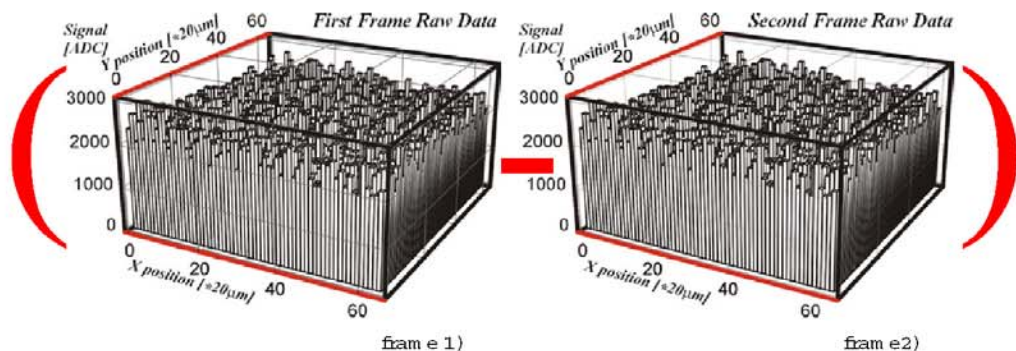
& storage

Low power – only significant draw at readout edge



Correlated Double Sampling

Data processing: (Digital) Correlated Double Sampling



Useful signal on top of
Fixed Pattern DC level

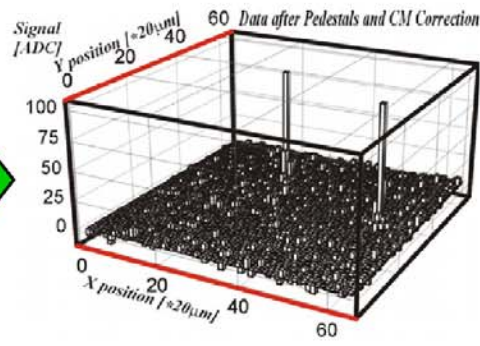
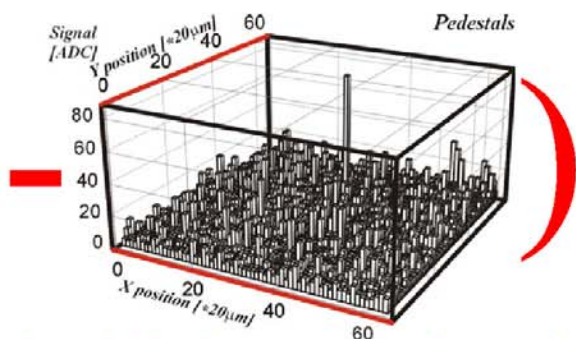
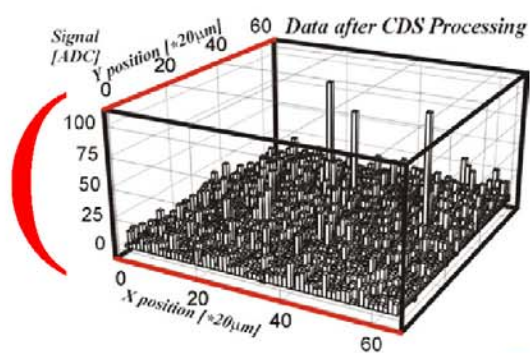
Fixed Pattern dispersion: ~ 100 mV

Typical signal amplitude: ~ 1 mV

(frame2 - frame1) subtraction



W. Dulinski [LEPSI]
MIMOSA4



Pedestal (dark current) subtraction

Hit candidates!



CAP1 Concept

- Automatic CDS – always sampling
 - When receive L1 trigger:
 - * sift data in sync pipe and provide the difference in value for orbit with trigger and preceding orbit
 - Analog reset
 - If reset once every 100 orbits, 1% “deadtime”
 - $1\mu\text{s}$ “reset” and $10\mu\text{s}$ to obtain a baseline sample
 - Possibly even less, depending upon dynamic range and background
 - Can build “intelligence” into reset
 - Minimization of leakage current important
 - Relatively simple to fabricate

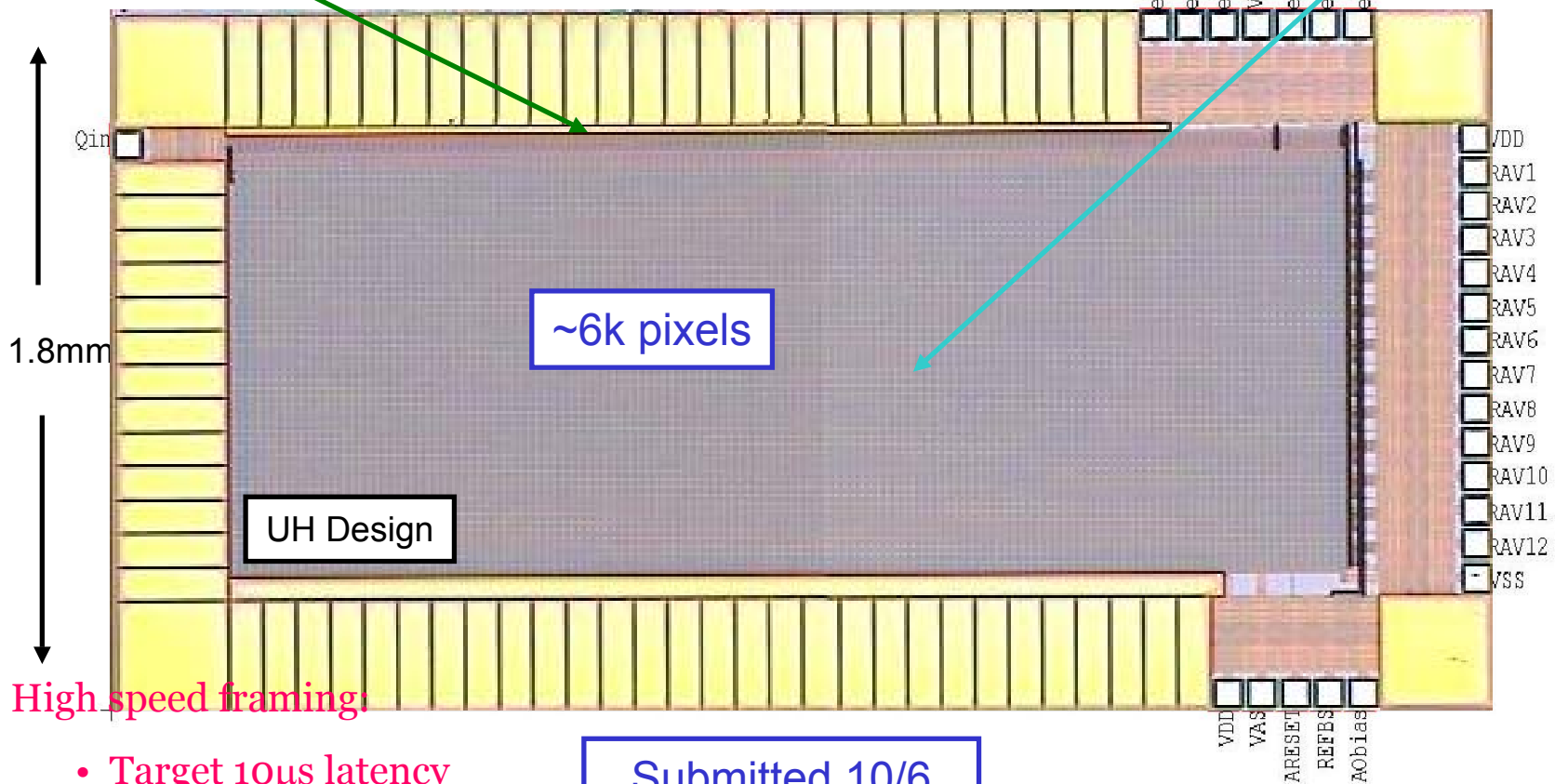


CAP1 Prototype

Column Ctrl Logic

• TSMC 0.35 μ m Process

132x48 (22.5 μ m² pixels)



Submitted 10/6
Received recently

"slow" readout resolution $\sim 2\mu$ m
At higher readout speeds?

• High speed framing!

• Target 10 μ s latency

• Pipelined readout



CAP2 Concept

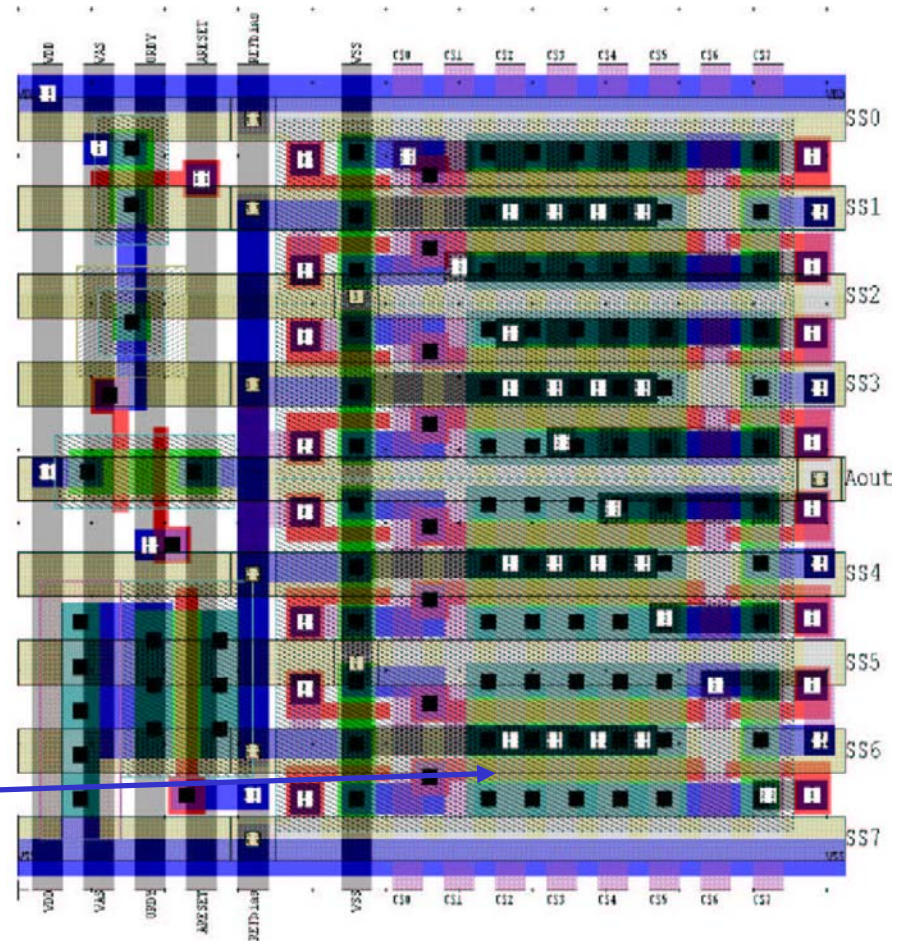
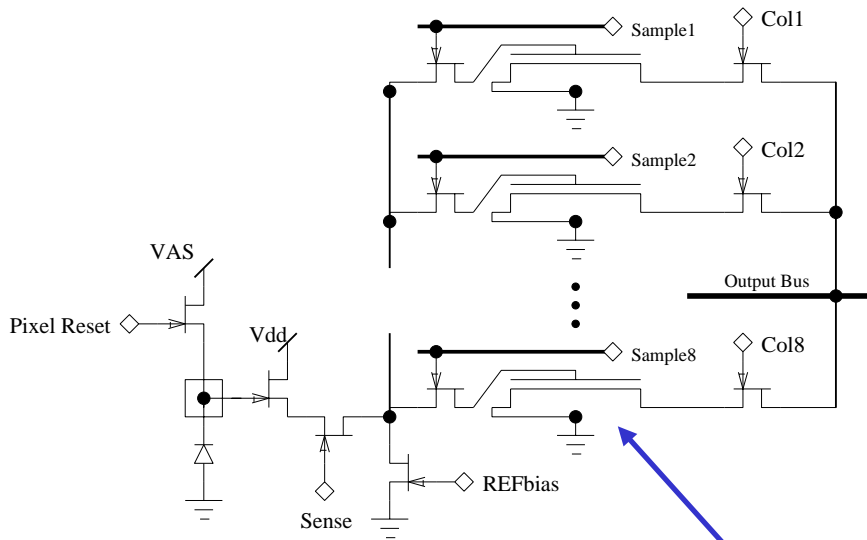
- CAP1 architecture difficulties:
 - Significant strain on analog output transfer:
 - <10ns settling time difficult
(will test, but SPICE simulation shows very marginal for full-sized detector)
 - Data volume reduction
 - Better if can provide true on-detector pipelining
 - Reduce power if constrict data flow to L1/L2 accepted events (100kHz → 10kHz or 1kHz):
40GSa/s → 4GSa/s or 0.4GSa/s

Possible to put a small pipeline in each pixel?



Octal-pipeline (in $22.5\mu\text{m}^2$ pixel)

Yes!
Random access, decoupled
Read/Write

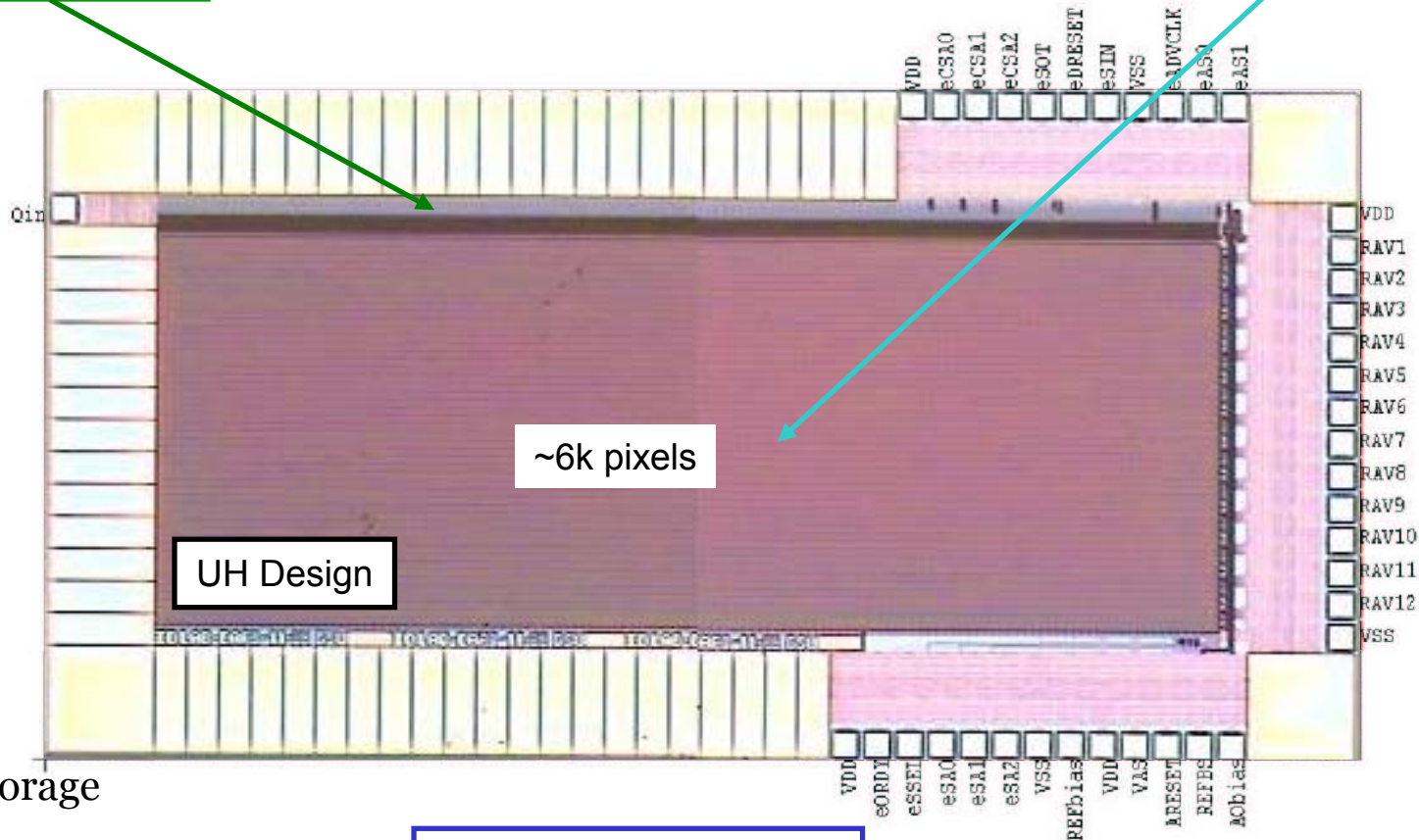


CAP2 Prototype

Column Ctrl Logic

• TSMC 0.35 μ m Process

132x48 (22.5 μ m² pixels)



1.8mm

~6k pixels

UH Design

• 8-deep storage

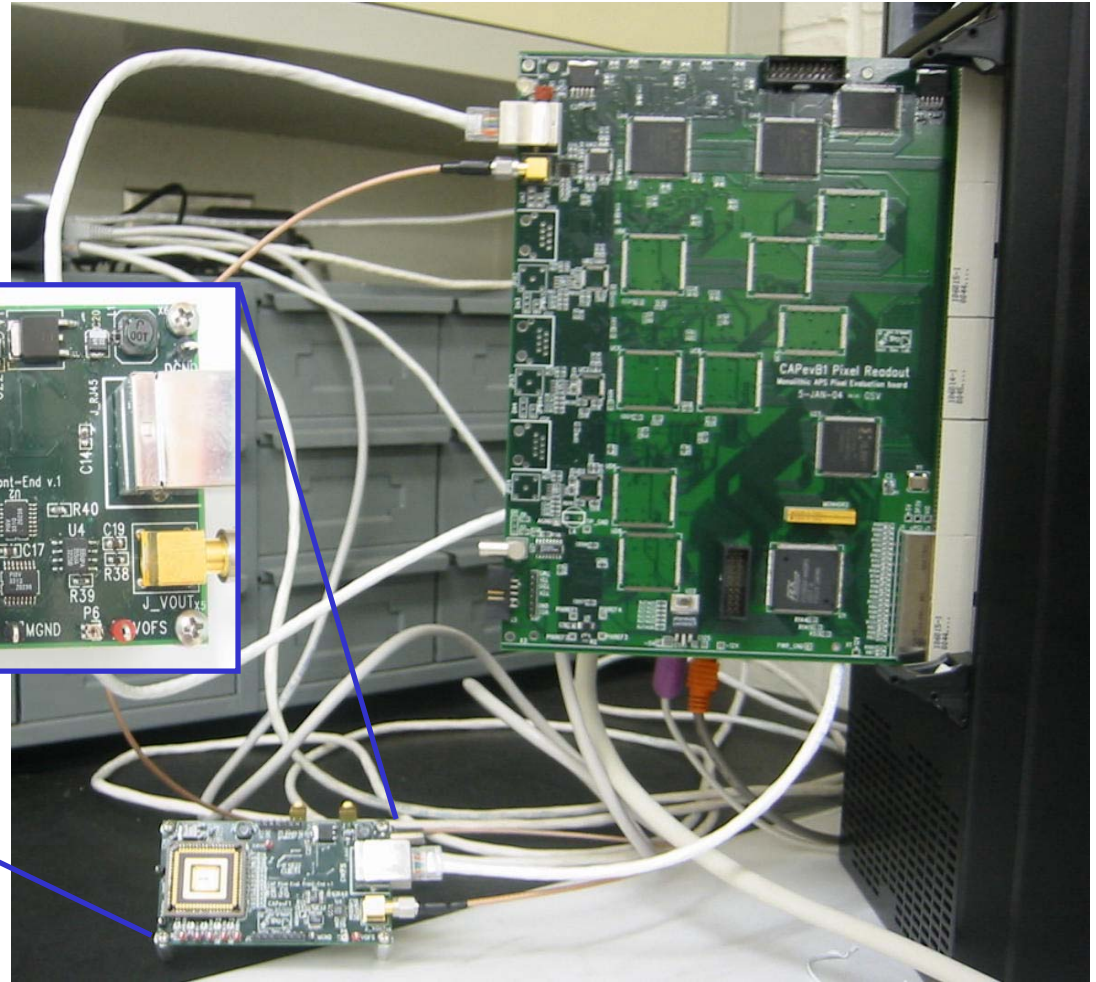
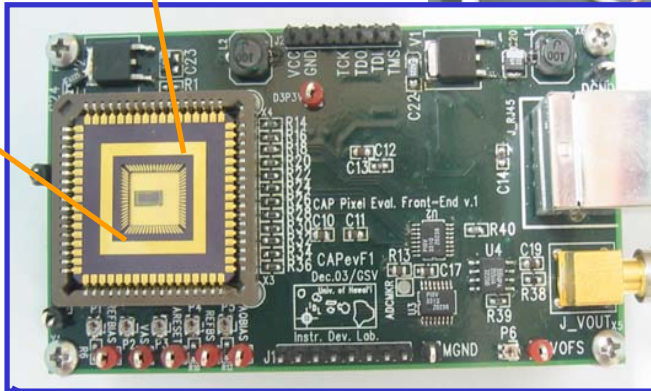
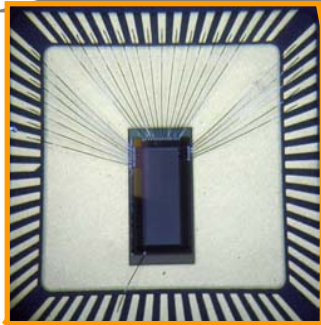
• Target 50 μ s latency

• Triggered readout

Submitted 10/27
Received last week



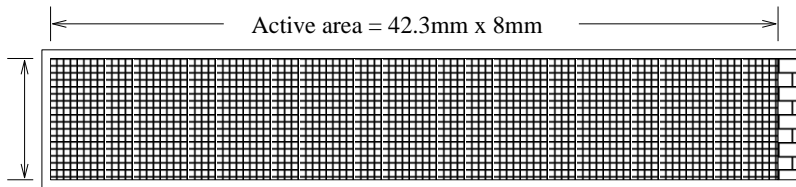
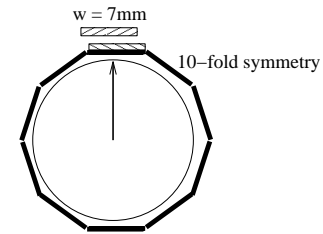
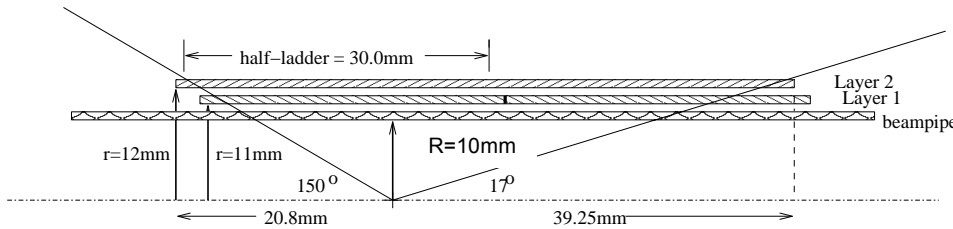
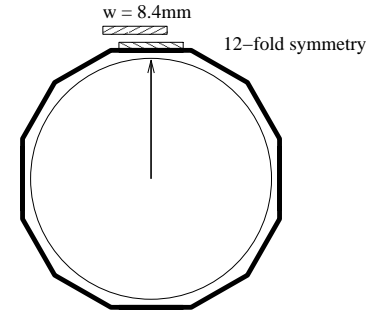
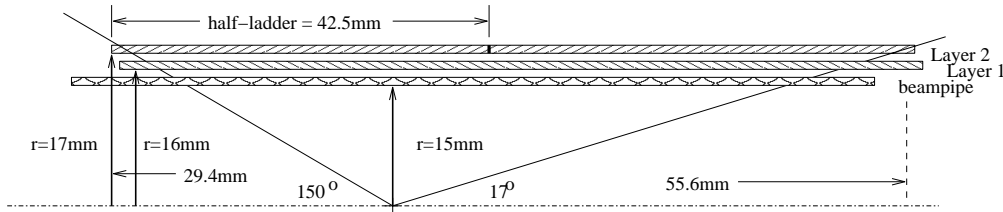
Prototype Test Bench



For those interested,
Will give a tour of the
ID Lab before lunch
Today



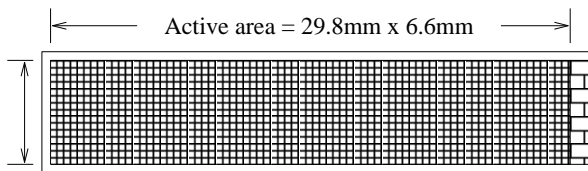
Straw-Man Channel Count



1880 x 356 = 669k channels

2 layers * 24 HL = 32M pixels

Half-ladders:



1324 x 293 = 388k channels

2 layers * 20 HL = 15.5M pixels



Occupancy Scaling

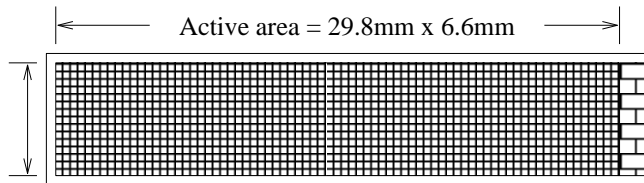
- Work from following assumptions:
 - Super-B canonical x20 background increase
 - Assume 10% Layer 1 occupancy as “current”
 - Strip area (L1) = 85mm x 50 μ m = 4.25M μ m²
 - Pixel spatial reduction:
 - Pixel area = 22.5 μ m x 22.5 μ m = 506 μ m²
 - Reduction factor ~8400
 - Pixel temporal loss:
 - 0.5 μ s SVD vs. 10 μ s PVD (could be improved)
 - Increase factor ~ 20
 - Grand total:
 - 10% * 20 * 8400⁻¹ * 20
 - Can expect ~ 0.5% occupancy



Event size

- Conservatively take 1% as Occupancy

R = 1cm case



1324 x 293 = 388k channels

155k Pixels

2 layers * 20 HL = 15.5M pixels

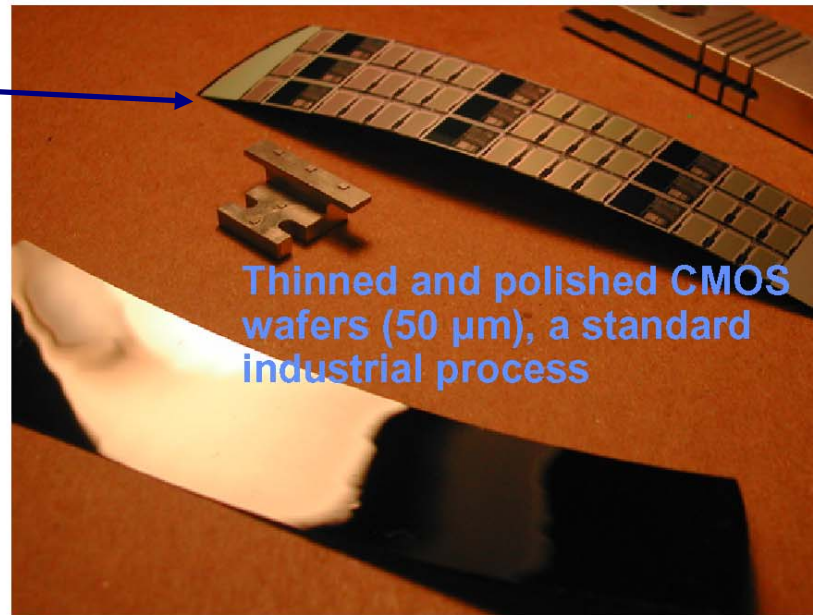
- 1 Byte/pixel (8bit ADC) sufficient
- **However**, need ~25 bits of address info
- 4 Bytes/pixel → 620kB/event
- Can reduce with clustering/track matching?



Thin is In

1. Thinning the substrate to $50\ \mu\text{m}$ (or less)
2. Low mass (air?) cooling: keeping down the power dissipation ($\sim 100\ \text{mW}/\text{cm}^2$)

LBNL old wafer

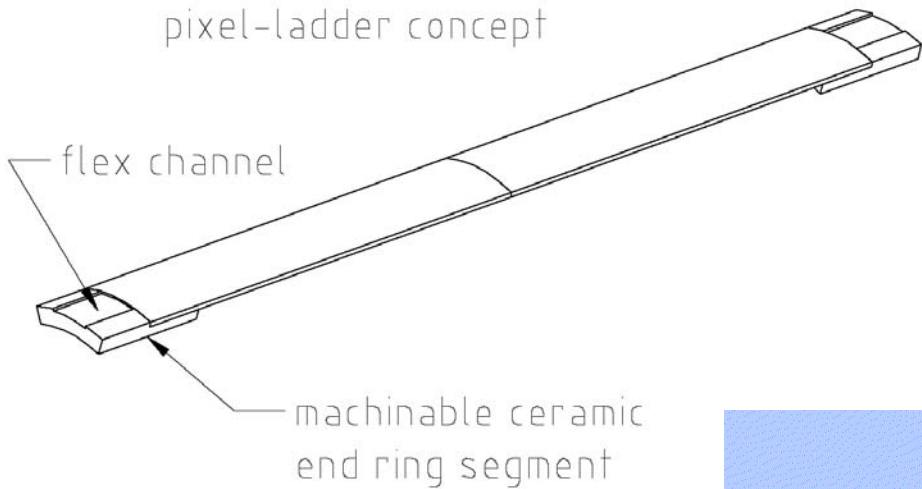


Starting to play with Samples @ UH

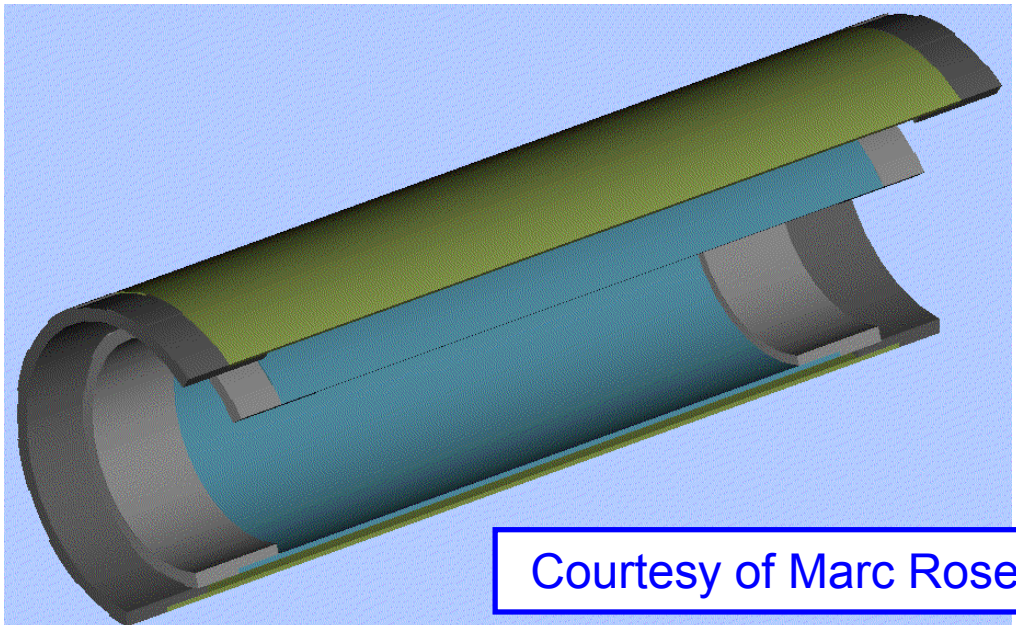
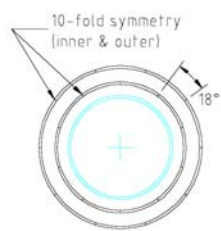
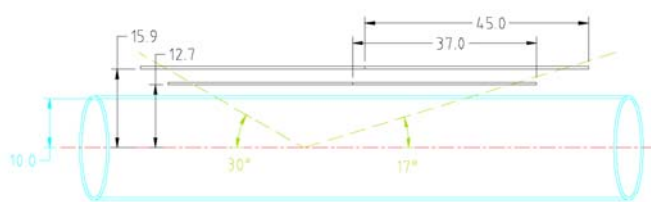


Detector Layout Concept

pixel-ladder concept



Significant Design Issues
But starting



Courtesy of Marc Rosen

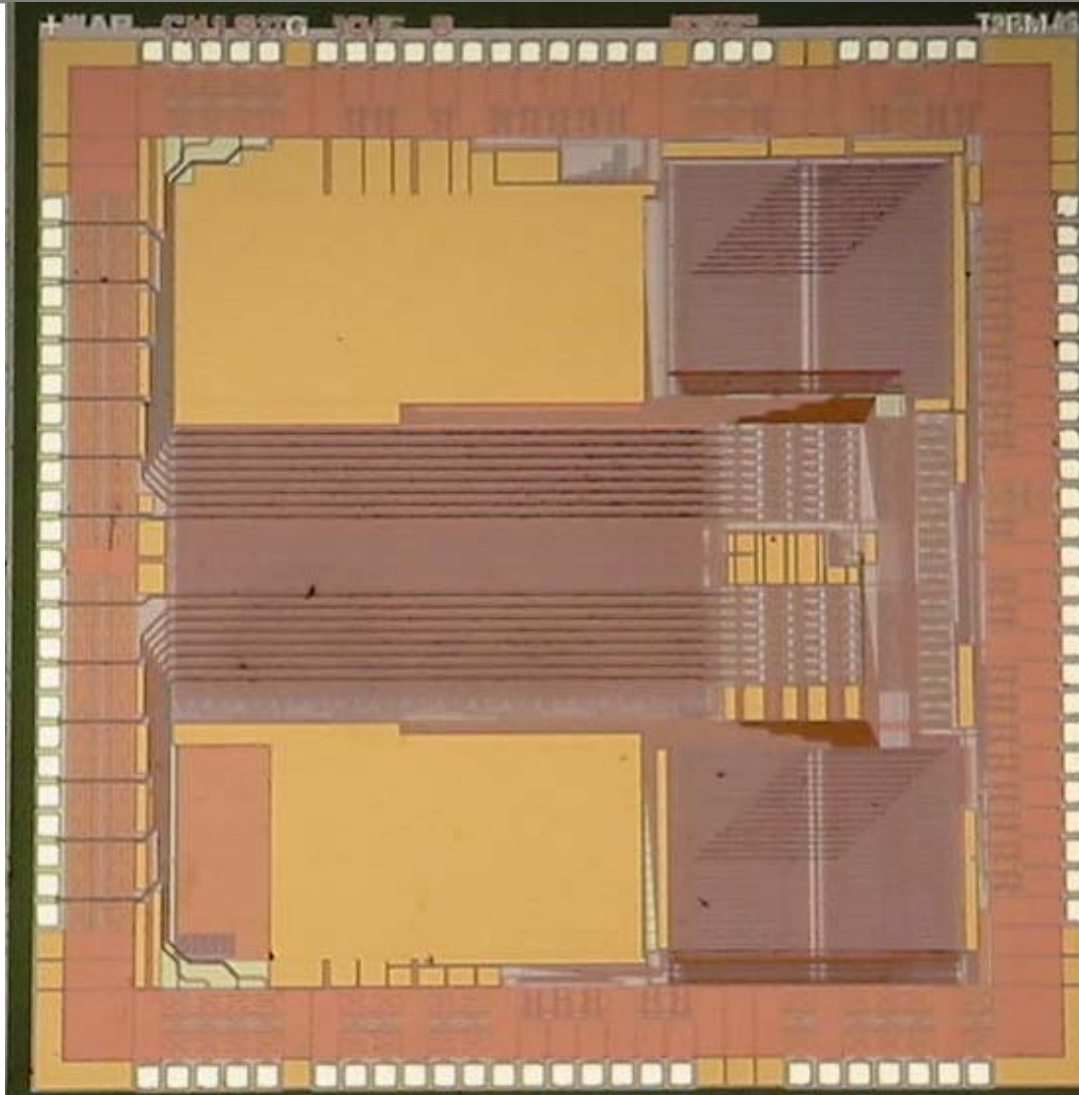


Summary

- Immediate Pixel Plans:
 - 2x prototypes fabricated by UH, full-size prototype in 2004 (after beam test)
 - SNR degradation at higher readout speeds
 - Leakage current @ large irradiation
 - Much effort required:
 - Enormous data volumes/bandwidth requirement
 - Support, stability and cooling of thin detector – without adding significant mass
 - Large data reduction possible – algorithms?
 - High speed test bench
- Longer-term R&D:
 - Possible BiCMOS (IBM SiGe) implementation of HS readout



Back-up slides

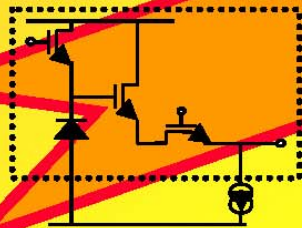


Yes! In fact not unique (RAL)

From PPARC Funding proposal request

Design for science-grade MAPS

Where we come from



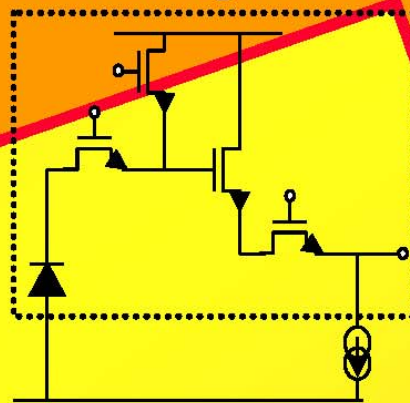
Consumer MAPS.

3 transistors

Simple, but high noise, no data processing, ...

Where we went from 2001 till now

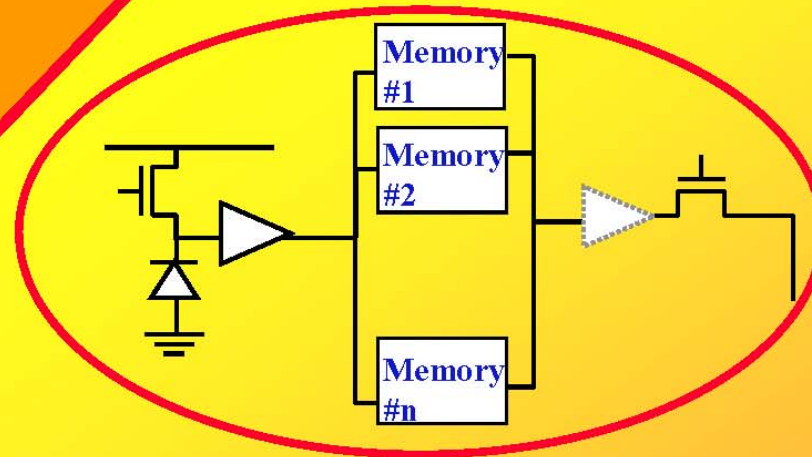
1st science-grade MAPS



4 transistors

Reduce kTC and fixed pattern noise, but still relatively slow and no data processing

Where we want to go
Flexible Active Pixel Sensors

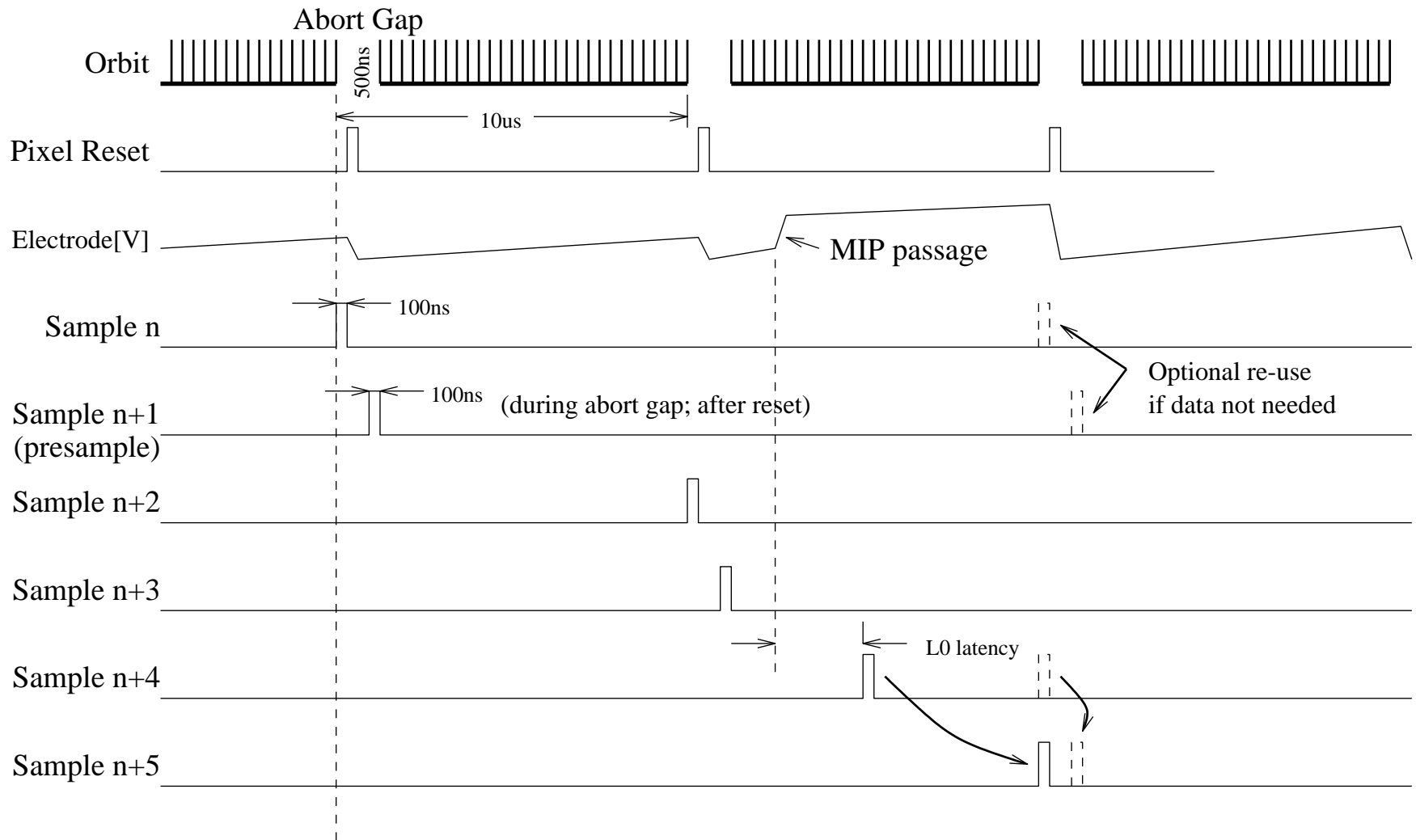


8 transistors + memory cells with storage and selection transistor

Very high speed, analogue data processing, reduced noise, necessary for particle physics applications

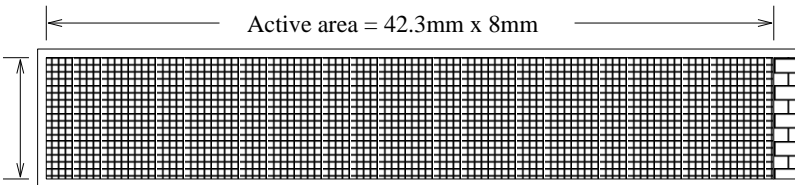


One Operating Mode



Event size

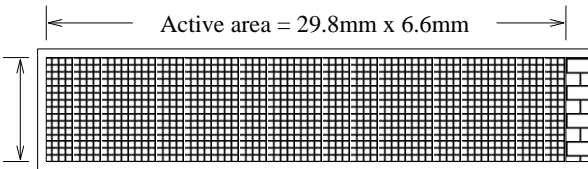
- Conservatively take 1% as Occupancy



1880 x 356 = 669k channels

2 layers * 24 HL = 32M pixels

320k Pixels



1324 x 293 = 388k channels

2 layers * 20 HL = 15.5M pixels

155k Pixels

- 1 Byte/pixel (8bit ADC) sufficient
- **However**, need ~25 bits of address info
- 4 Bytes/pixel → 620-1280kB/event
- Can reduce with clustering/track matching?



Required Transfer Rates

- CAP1 architecture (if $10\mu\text{s}$ max. latency):

- 15mm radius:

- 67 Gpixels/s
- $\sim 1\text{Gpixel/s/pin}$

- 10mm radius

- 39 Gpixels/s
- $\sim 0.5\text{Gpixel/s/pin}$

Two ways around:
- Multi-orbit
- “Tiling”

- CAP2 architecture ($\geq 100\mu\text{s}$ max. latency):

- 15mm radius:

- 6.7 Gpixels/s
- $\sim 100\text{Mpixel/s/pin}$

- 10mm radius

- 3.9 Gpixels/s
- $\sim 50\text{Mpixel/s/pin}$

Real max. latency
Set by $\langle L1/L2 \rangle$ rate



The Bottleneck

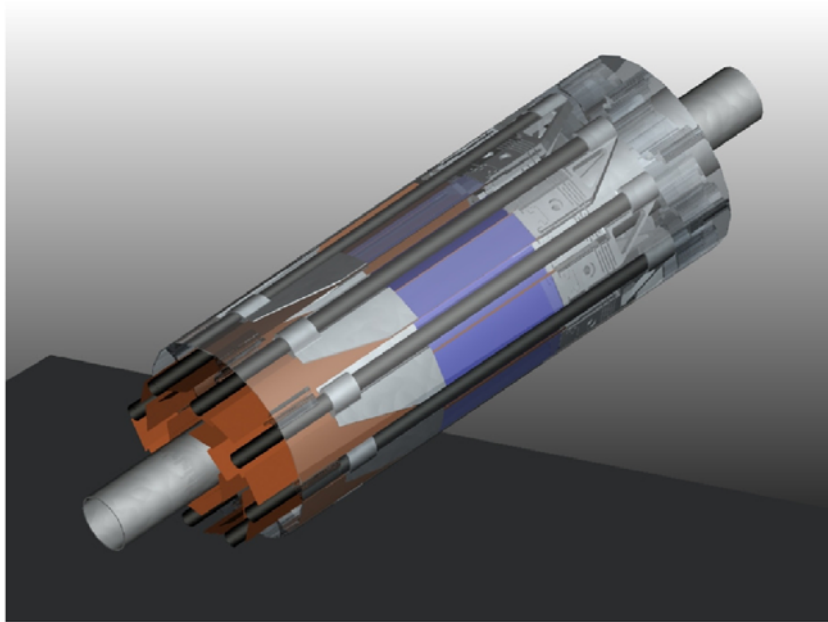
- Not trivial, but probably possible to:
 - Sample with adequate SNR
 - Read data off pixel with small enough latency
 - Provide periodic analog resets without incurring deadtime
- However:
 - Not easy to get this torrent to the electronics hut
 - Exploring 2 different fiber optics schemes
 - Custom SiGe mixer/modulator may be a solution
- Looks like can fit everything in one COPPER crate:
 - 1 high-speed fiber/half ladder
 - 1 high-speed fiber/FINESSE
 - Each FINESSE does all CDS/offset calculations
 - CPU does clustering?



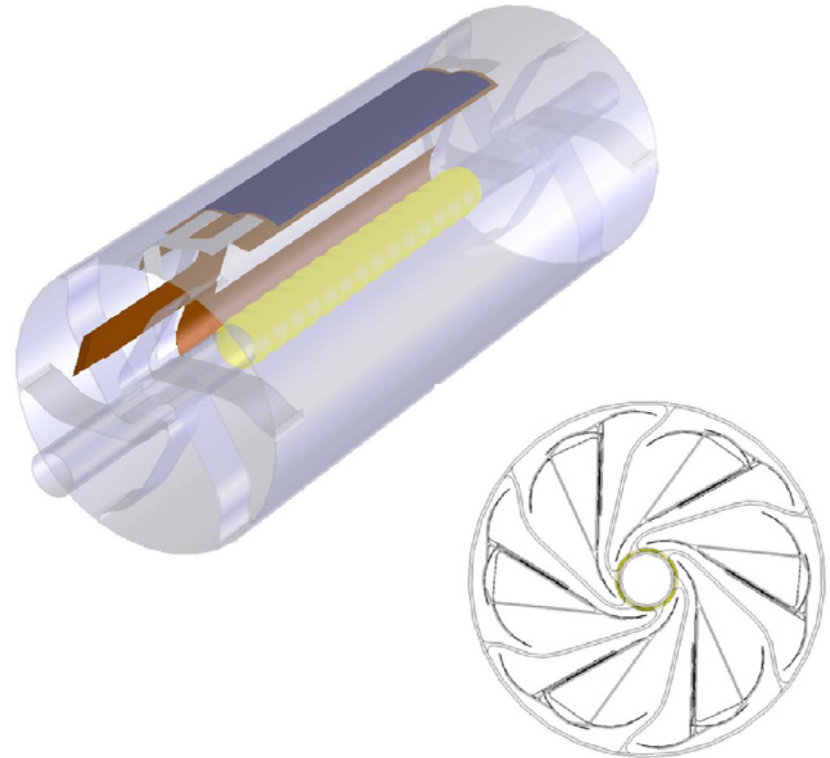
Mechanics

Very preliminary

Mechanical concepts of STAR Micro vertex upgrade using ultra-thin CMOS MAPS *



Tension concept



Self supporting Venetian blade concept

* Curtsey to Howard Wieman, LBL, STAR group

