

Belle Monolithic Thin Pixel Upgrade -- Update

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On Behalf of the Pixel Gang
(Marlon, Fang, ...)
Local Belle Meeting
March 2004
Univ. of Hawaii



Today's delta

- Have shown basic scheme before
 - Testing has really started
 - Many thanks to Fang and Marlon
- CAP1 Results
 - Cosmic muon testing
 - * Continuing to improve SNR
 - Radioactive sources
 - Excellent confirmation of rate
- What's next

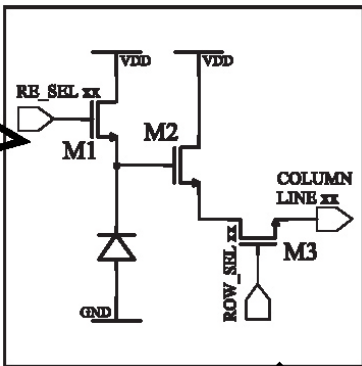


Continuous Acquisition Pixel

- Conceptually Simple

- Analog reset, sample & then sample continuously
- Row-wise analog shift out as fast as possible:

- Consider $22.5\mu\text{m}$ pitch output w/ 4:1 AMUX
- 100MSa/s output (e.g. 8-bit ADC on output)
- $10\mu\text{s}$ for 1k columns (# row independent)
- Possibility of passing signals through to allow joining to form ladders

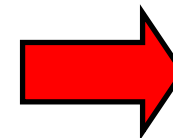


Standard APS pixel



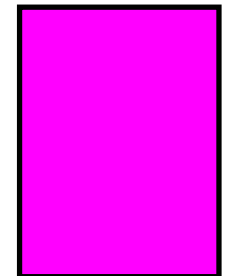
Pixel Array: Column select – ganged row read

High-speed



analog

ADC



& storage

Low power – only significant draw at readout edge

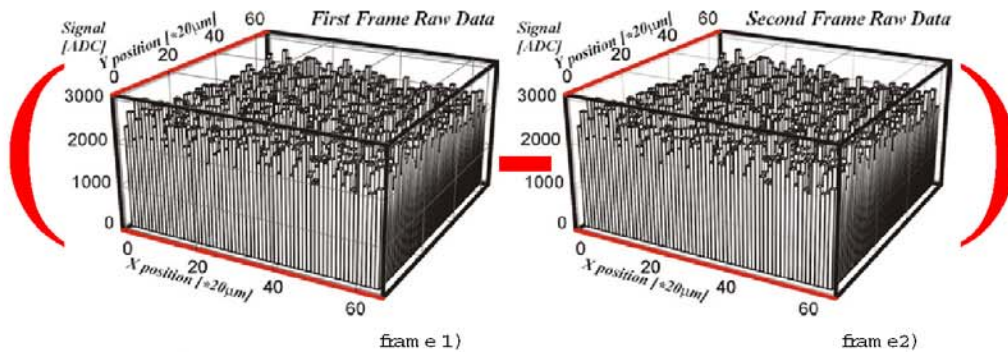
CAP1 Concept

- Automatic CDS – always sampling
 - When receive L1 trigger:
 - * sift data in sync pipe and provide the difference in value for orbit with trigger and preceding orbit
 - Analog reset
 - If reset once every 100 orbits, 1% “deadtime”
 - $1\mu\text{s}$ “reset” and $10\mu\text{s}$ to obtain a baseline sample
 - Possibly even less, depending upon dynamic range and background
 - Can build “intelligence” into reset
 - Minimization of leakage current important
 - Relatively simple to fabricate



Correlated Double Sampling

Data processing: (Digital) Correlated Double Sampling

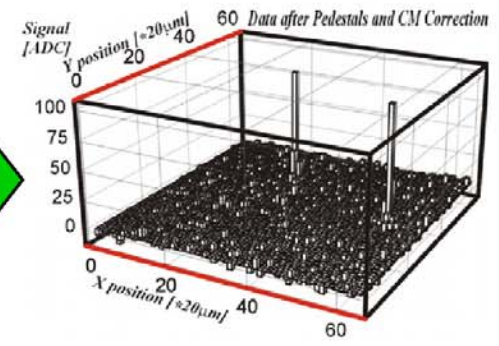
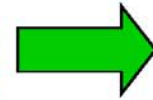
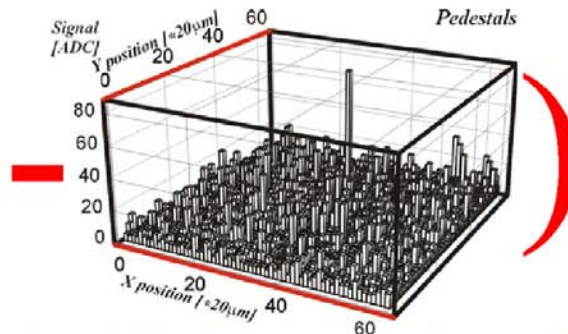
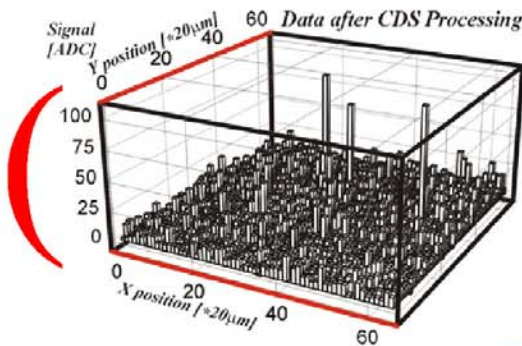


Useful signal on top of
Fixed Pattern DC level

Fixed Pattern dispersion: ~100 mV

Typical signal amplitude: ~1mV

(frame2 - frame1) subtraction



Pedestal (dark current) subtraction

Hit candidates!

W. Dulinski [LEPSI]
MIMOSA4

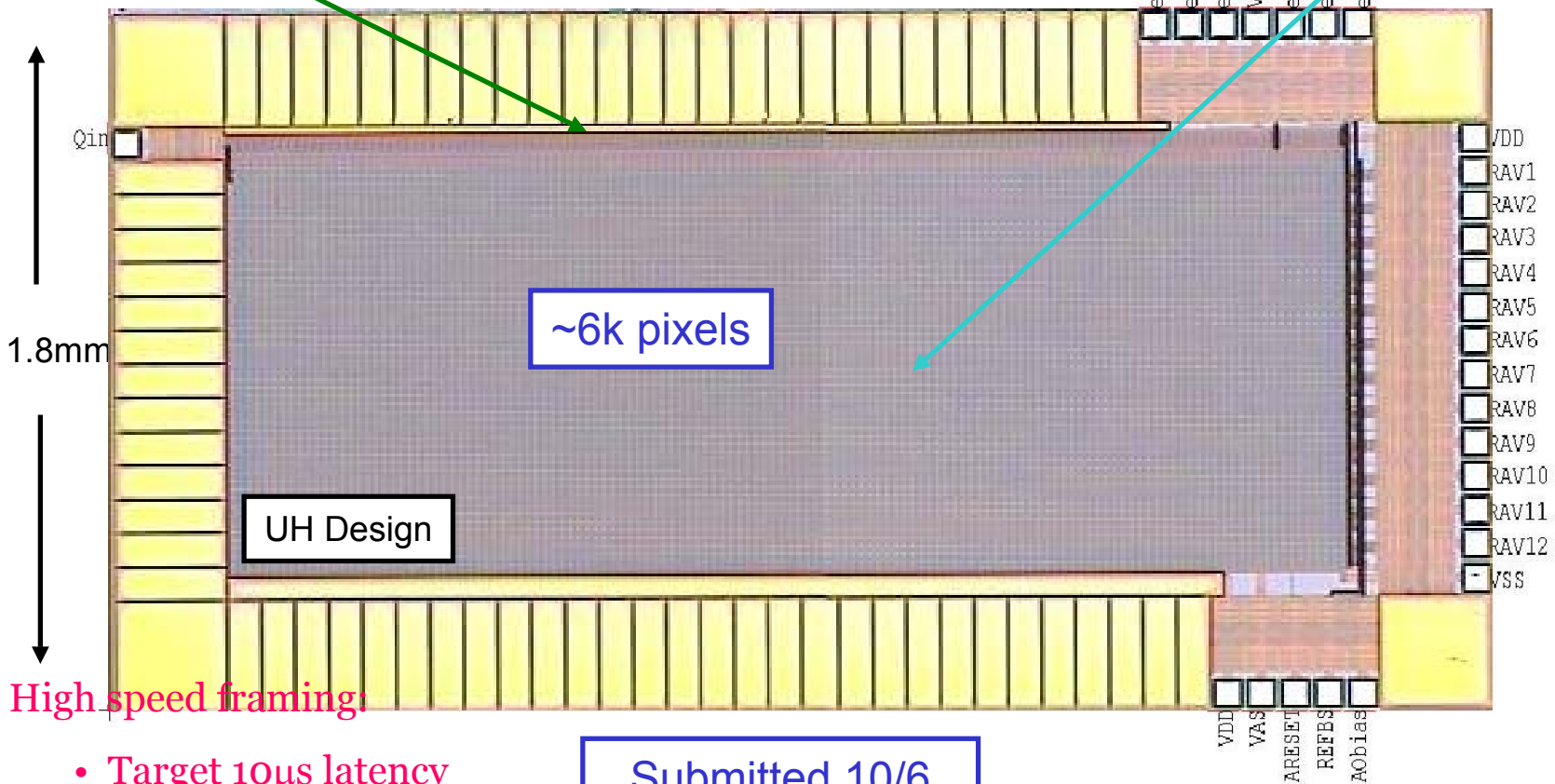


CAP1 Prototype

Column Ctrl Logic

• TSMC 0.35 μ m Process

132x48 (22.5 μ m² pixels)



~6k pixels

UH Design

1.8mm

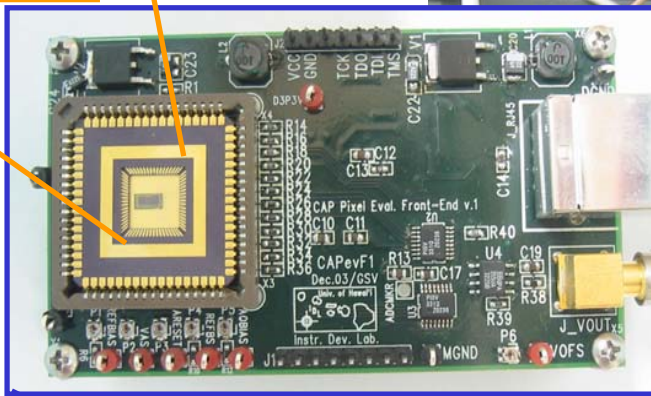
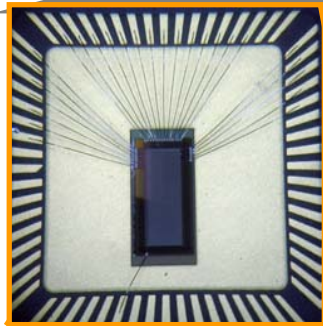
Submitted 10/6
Received recently

“slow” readout resolution ~ 2 μ m
At higher readout speeds?

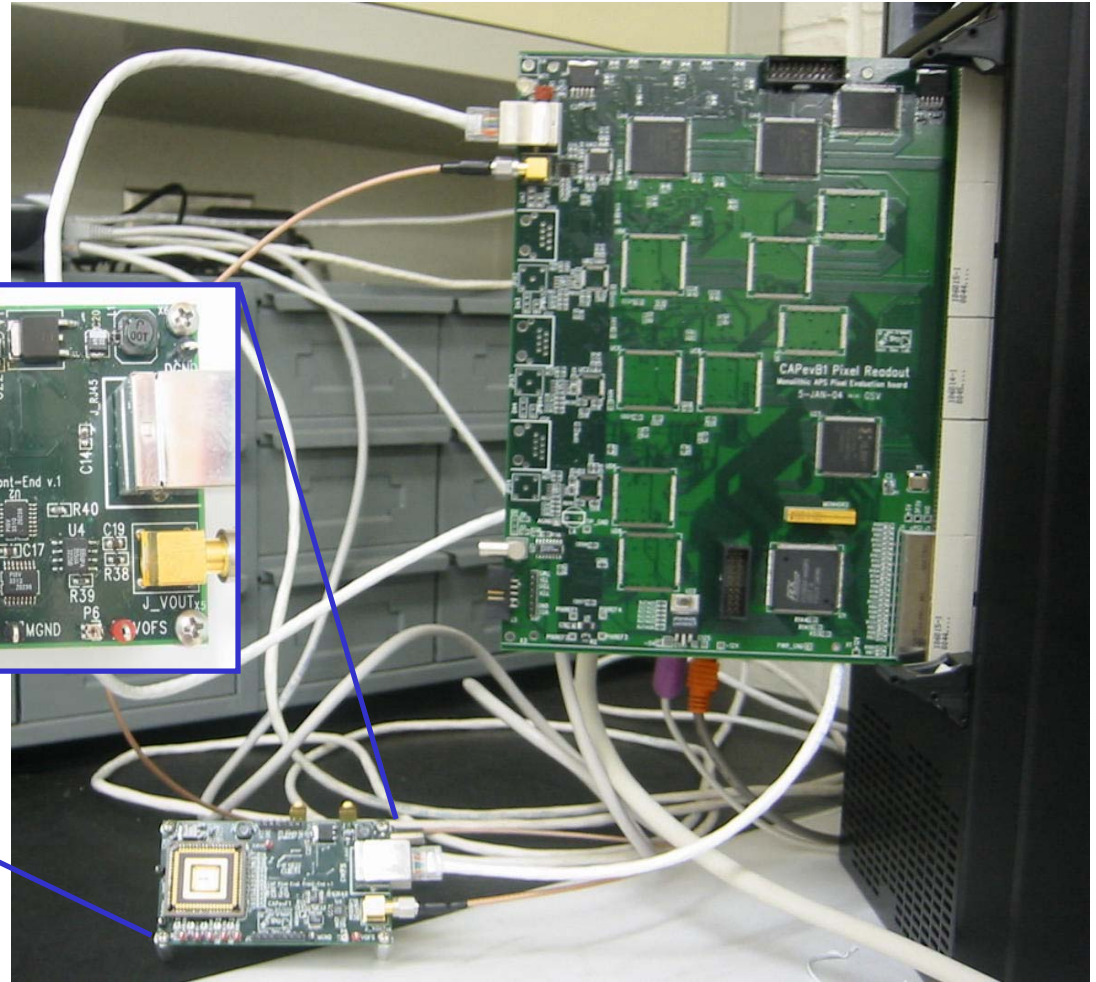
- High speed framing
- Target 10 μ s latency
- Pipelined readout



Prototype Test Bench



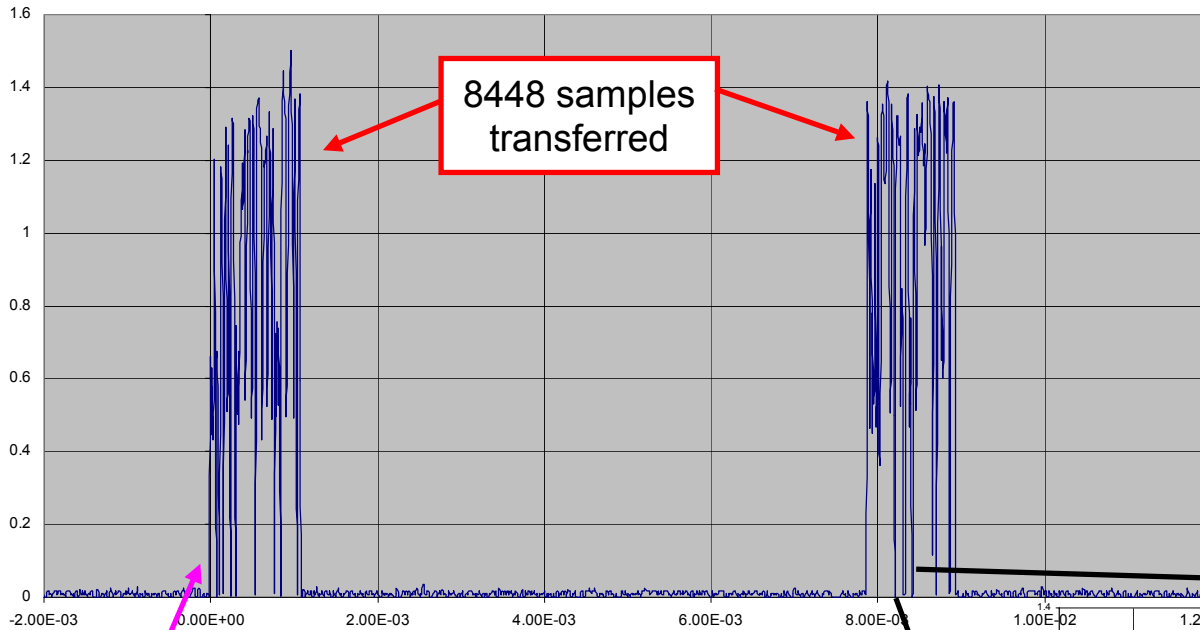
Compact PCI (cPCI)
based



Cosmic Sampling Cycle

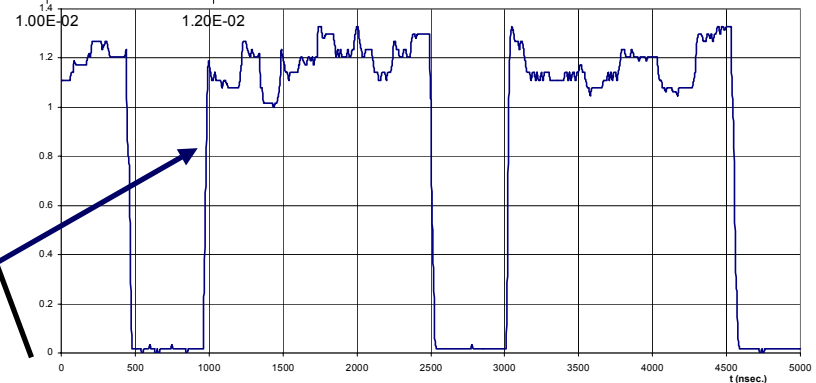
Pixel array complete acquisition (fr1/fr2)

~33ms cycle
~30 Hz acquisition



50 ohm cable settling time dominated

Pixel Readout Structure

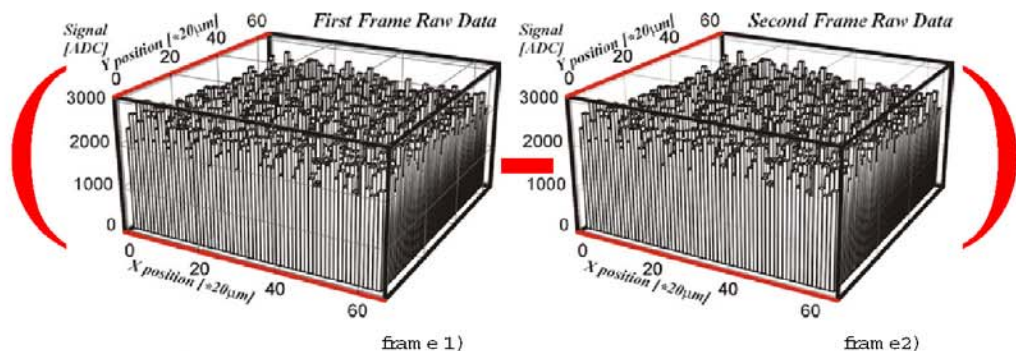


Analog reset

8MSa/s readout

Correlated Double Sampling

Data processing: (Digital) Correlated Double Sampling



Useful signal on top of
Fixed Pattern DC level

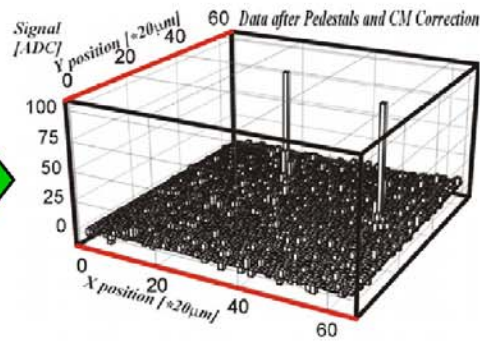
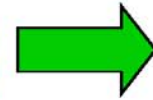
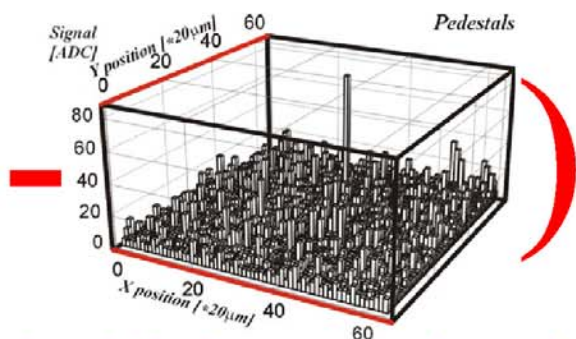
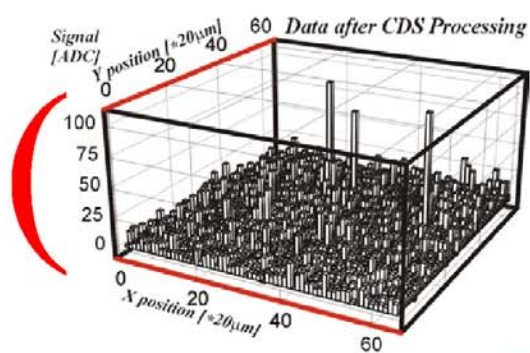
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(frame2 - frame1) subtraction



W. Dulinski [LEPSI]
MIMOSA4

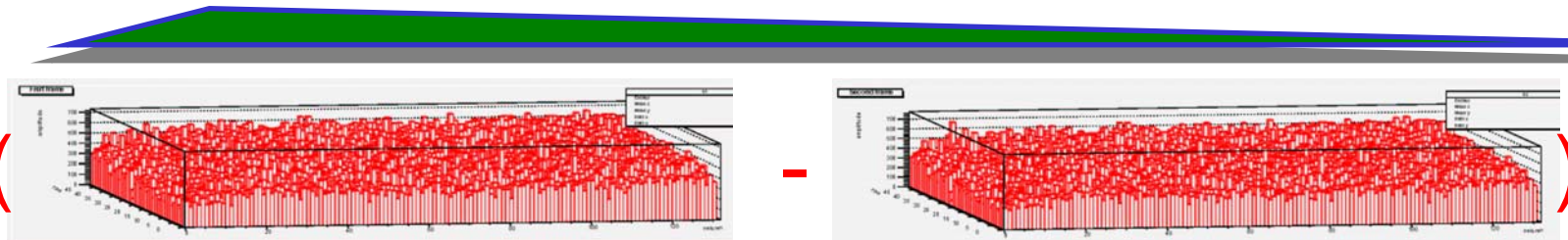


Pedestal (dark current) subtraction

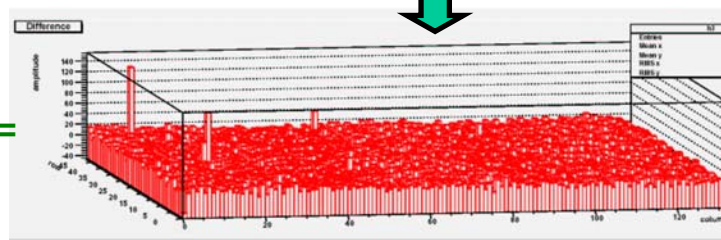
Hit candidates!



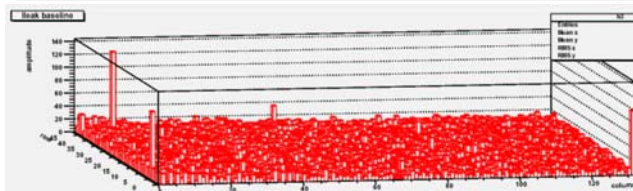
CAP CDS



Frame 1 - Frame 2 =



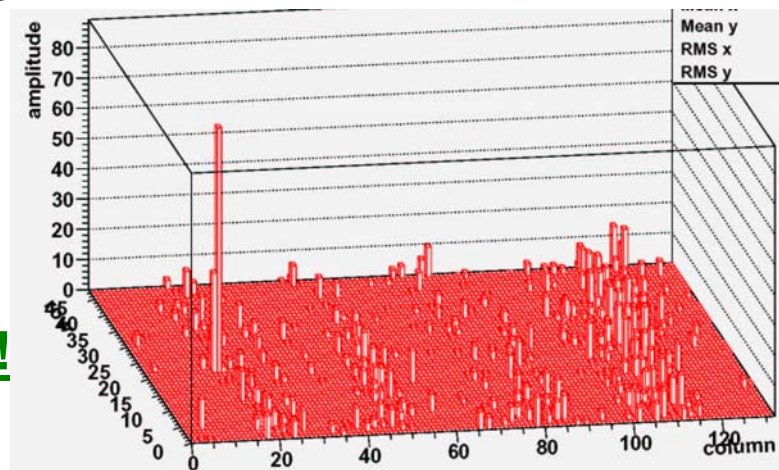
- Leakage current Correction



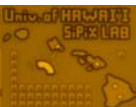
8ms integration

Can readout/process @ 30Hz – 25% livetime

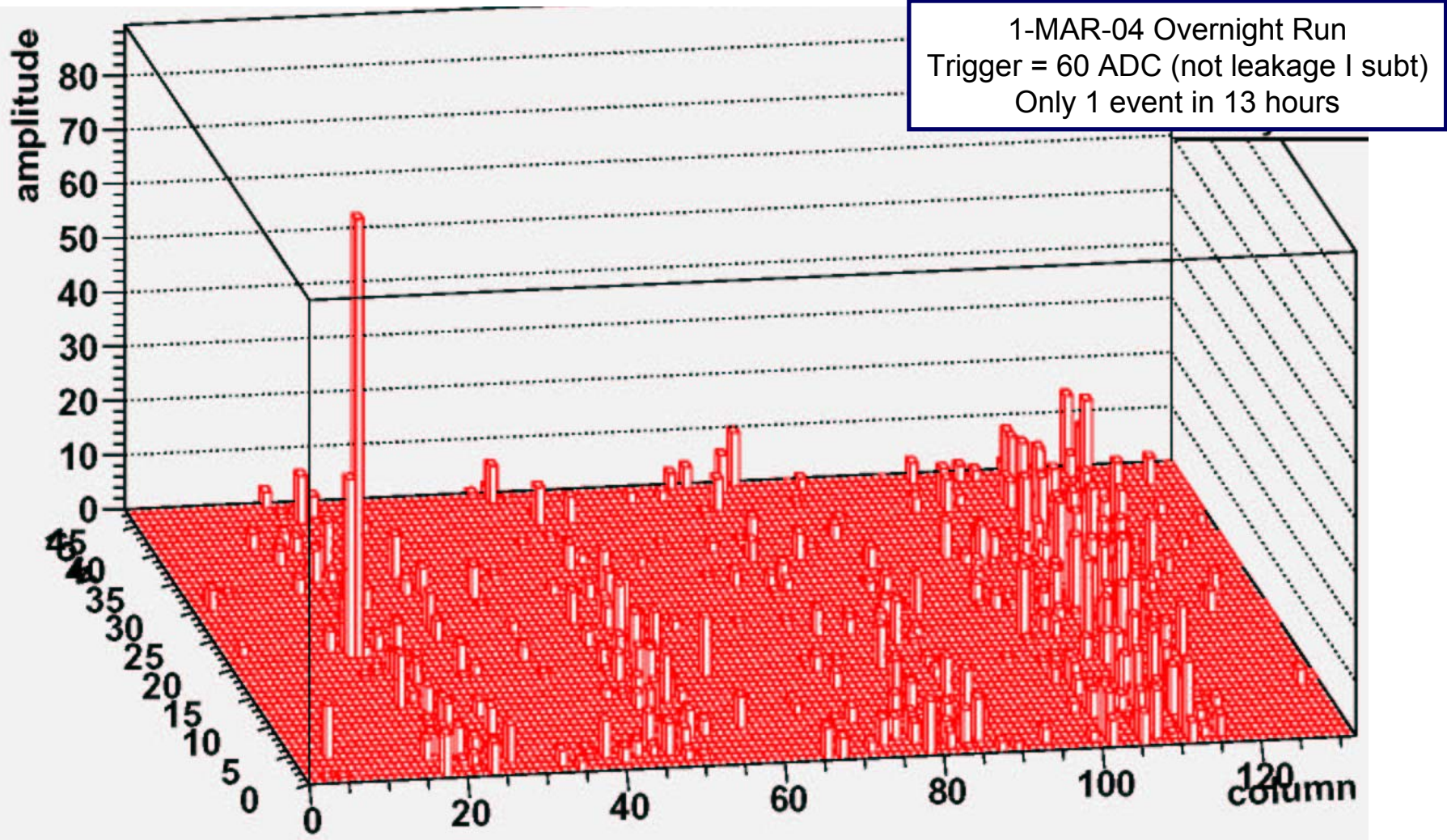
~fA leakage current (typ)
~18fA for hottest pixel shown



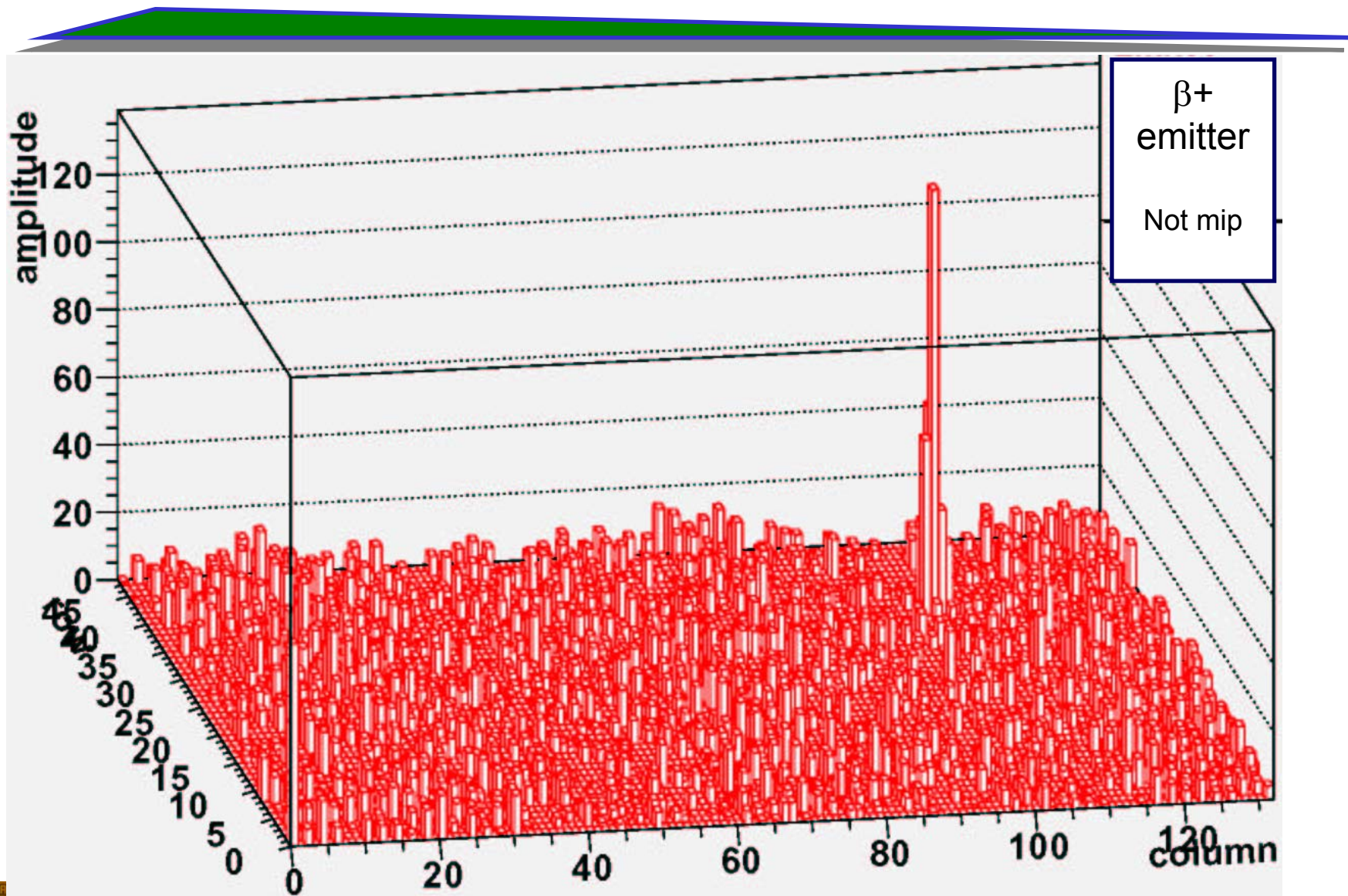
Cosmic muon candidate!



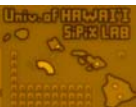
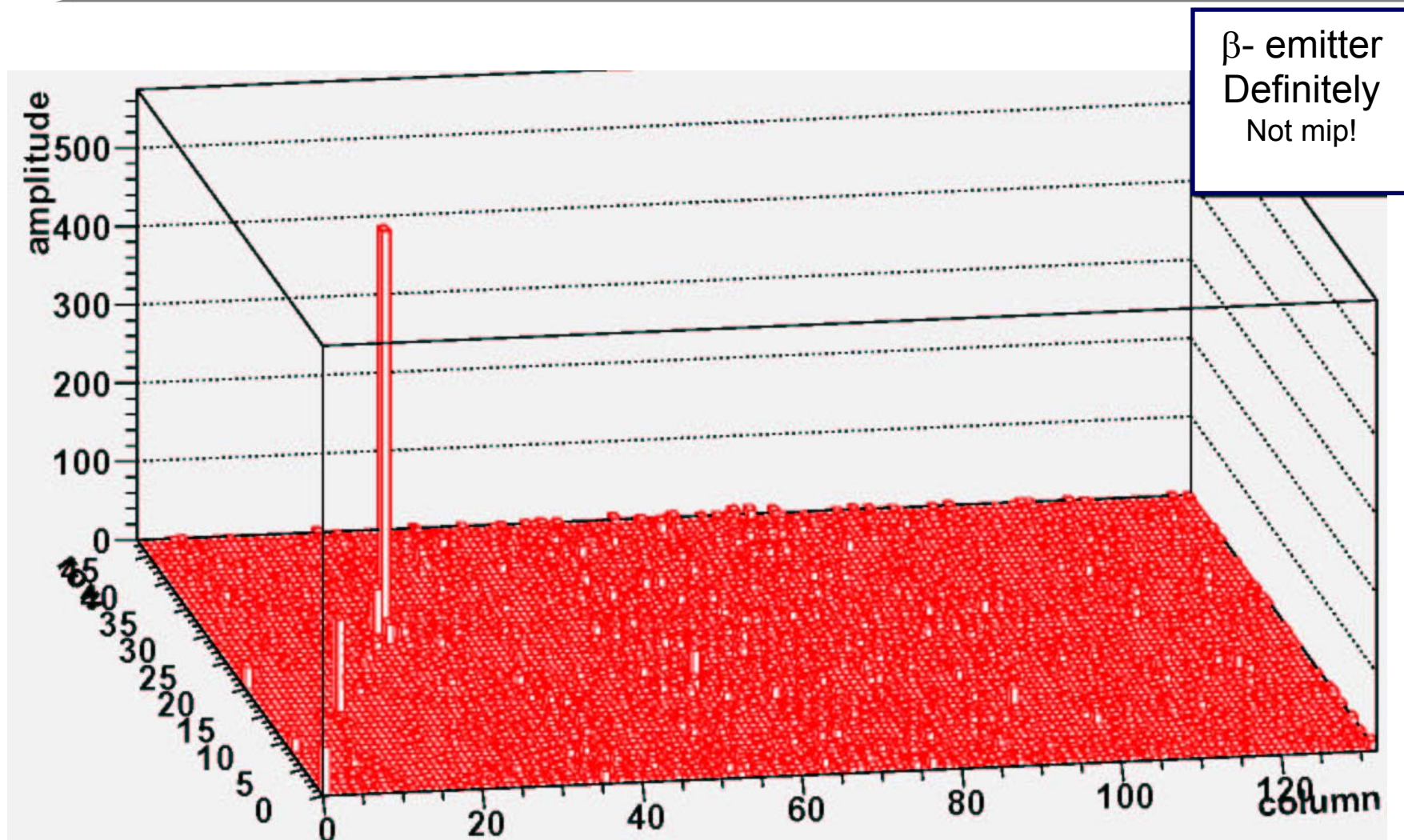
First Cosmic Event



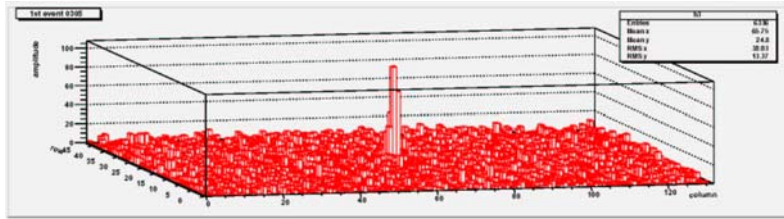
Source Check – Na22



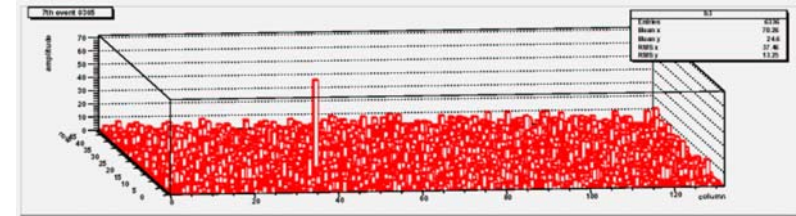
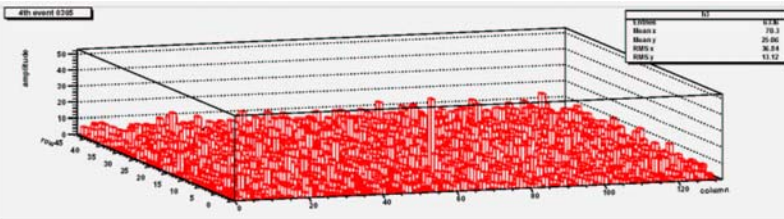
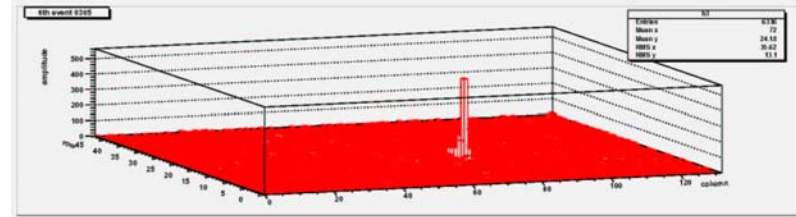
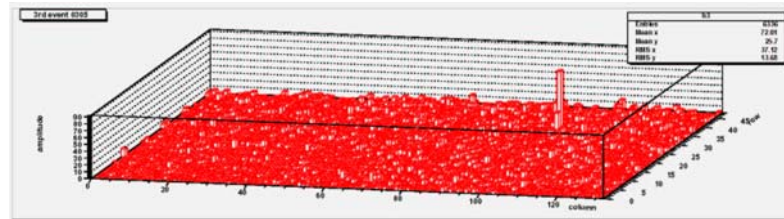
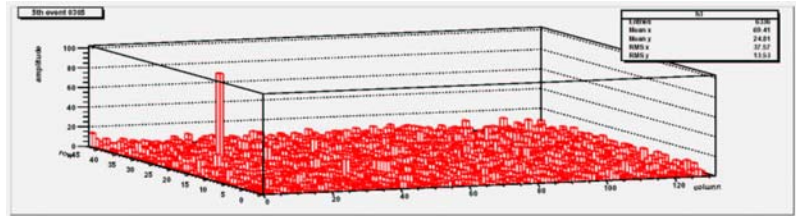
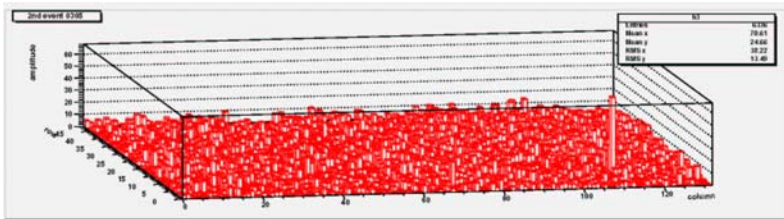
Source Check – Cs137



Continuing Cosmics



4-MAR-04 Overnight Run
 Trigger = 45 ADC counts
 7 events – much better noise



SNR Comparison

SPICE extraction:	3.22 fF	+/- 0.6fF?	Detector:	14 μ m			
Q=	1.60E-19 C/e-	Q=C*V	DSSD ref:	300 μ m	24000	e-hole pair/m.l.p.	
V=	4.97E-05 V/e-		Geom SF:	0.046667			
chip transfer: (SPICE)	0.78	Vout/Vin	Signal:	1120 e-	max produced		
Resistive Divider:	1	was 2:1	Collection efficiency	0.5	w.a.g. -- in max channel		
CAPevF1 amp:	7	gain	Peak signal:	560 e-			
50 ohm series term:	0.5	voltage divide					
CAPevB1 amp:	0.65	gain					
Net transfer gain:	1.7745						
Sensitivity:	0.088174	mV/e-	Expected SNR:	16.45913			
CAPevB1 noise:	3	ADC lsb noise	Sigma Set:	7			
CAPevB1 ADC:	1	mV/lsb	Threshold:	60			
CAPevB1 sensitivity:	11.34122	e-/lsb	m.l.p exp.	49.37739			
CAPevB1 floor:	34.02367	e-					



What's Next

- Short term goals:
 - Multiple detector operation
 - Hardware in hand
 - A bit of firmware, soldering yet required
 - CAP2 Evaluation
 - Use CAP1 as a trigger (?)
 - Possibility of very fast sampling
 - Mean, sigma statistics
 - Fang working on
 - Interactive event display (online vs. offline)
 - Beamtest box
 - Fine alignment of multiple CAP1/CAP2 for testing
 - Dark box to avoid heavy metal covers
 - Within a month or two could be ready for BOO

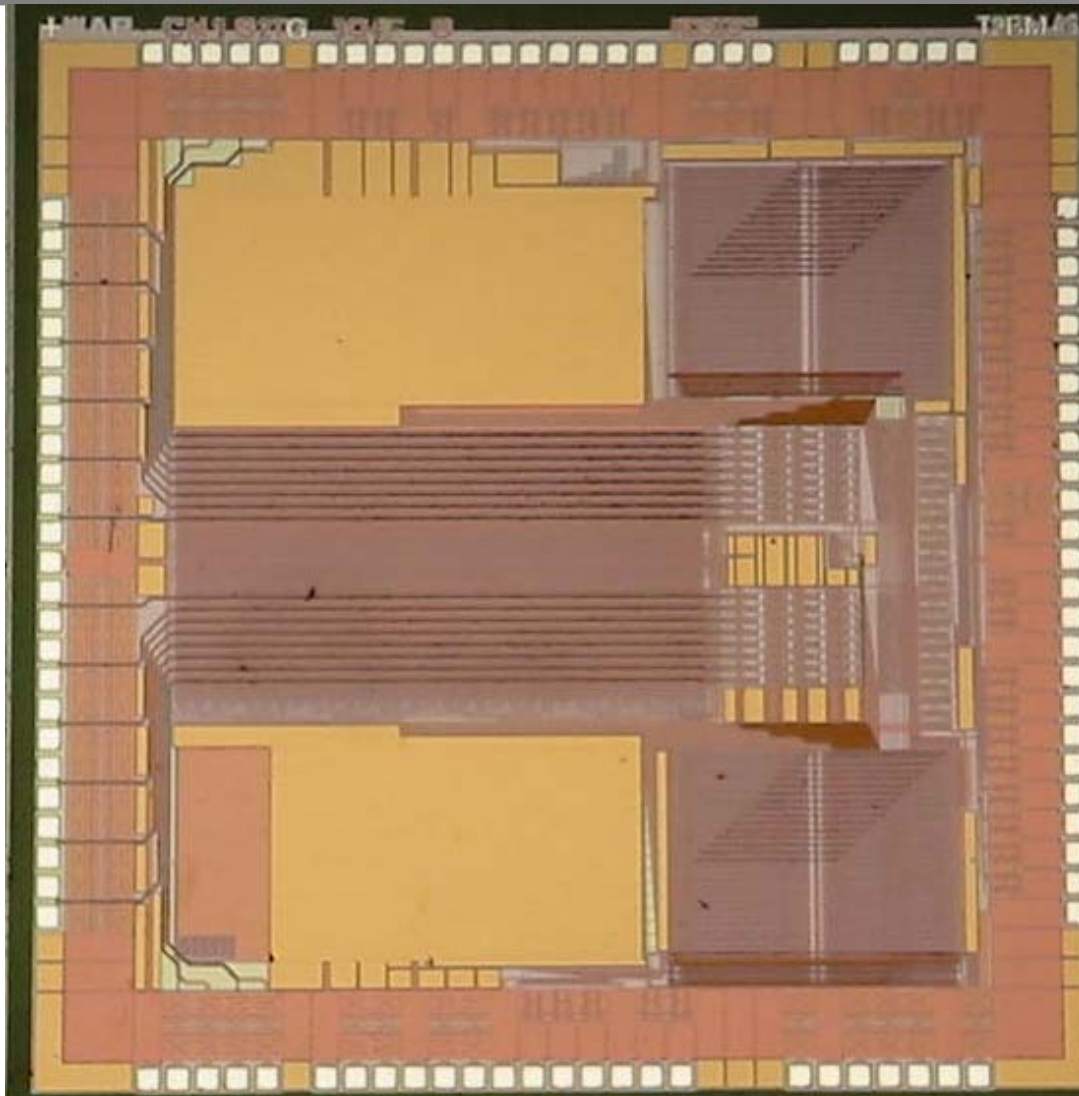


Summary

- Thanks to Marlon and Fang's efforts:
 - On track toward summer beam test
 - SNR optimization
 - Leakage current @ large irradiation (during BGM)
 - Alignment needs work
 - Much effort required:
 - Enormous data volumes/bandwidth requirement
 - Support, stability and cooling of thin detector – without adding significant mass
 - Large data reduction possible – algorithms?
 - Opportunities to participate available now
- Beam Test:
 - All welcome – please plan to join



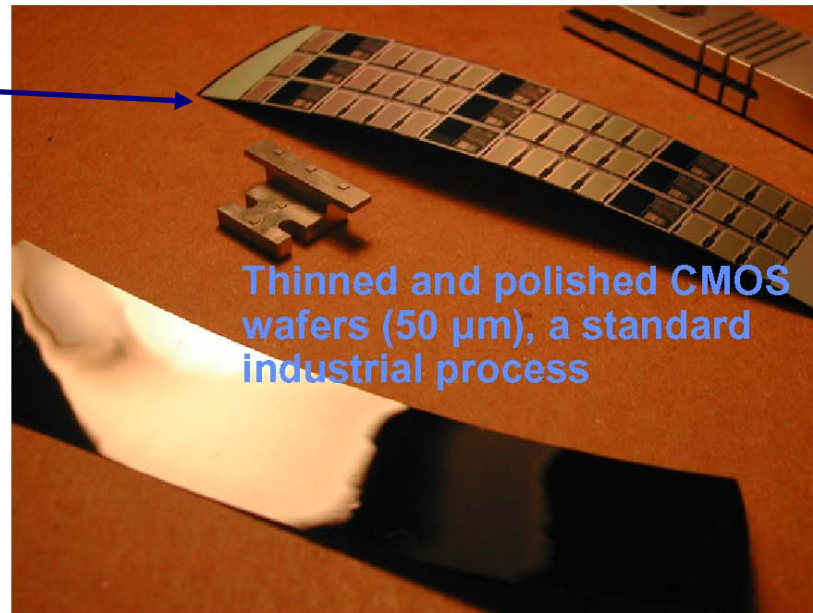
Back-up slides



Thin is In

1. Thinning the substrate to 50 μm (or less)
2. Low mass (air?) cooling: keeping down the power dissipation ($\sim 100 \text{ mW/cm}^2$)

LBNL old wafer



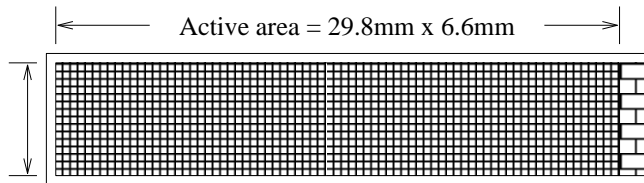
Starting to play with Samples @ UH



Event size

- Conservatively take 1% as Occupancy

R = 1cm case



1324 x 293 = 388k channels

155k Pixels

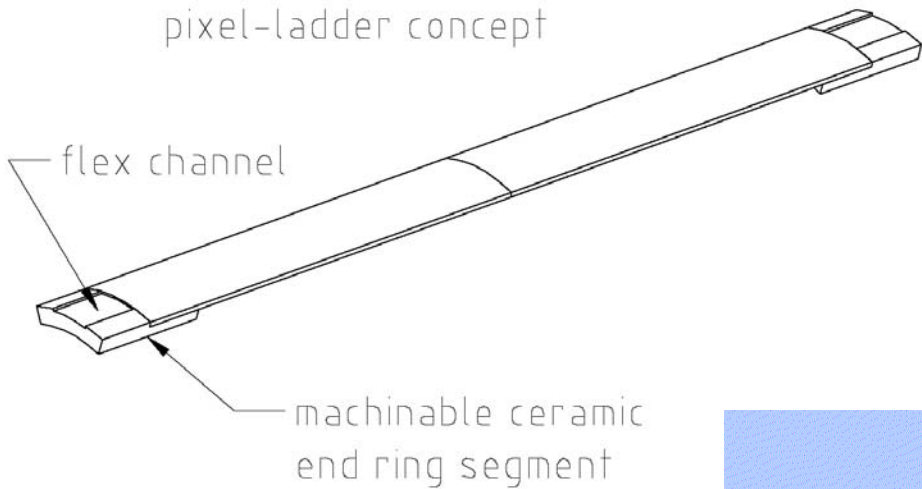
2 layers * 20 HL = 15.5M pixels

- 1 Byte/pixel (8bit ADC) sufficient
- **However**, need ~25 bits of address info
- 4 Bytes/pixel → 620kB/event
- Can reduce with clustering/track matching?

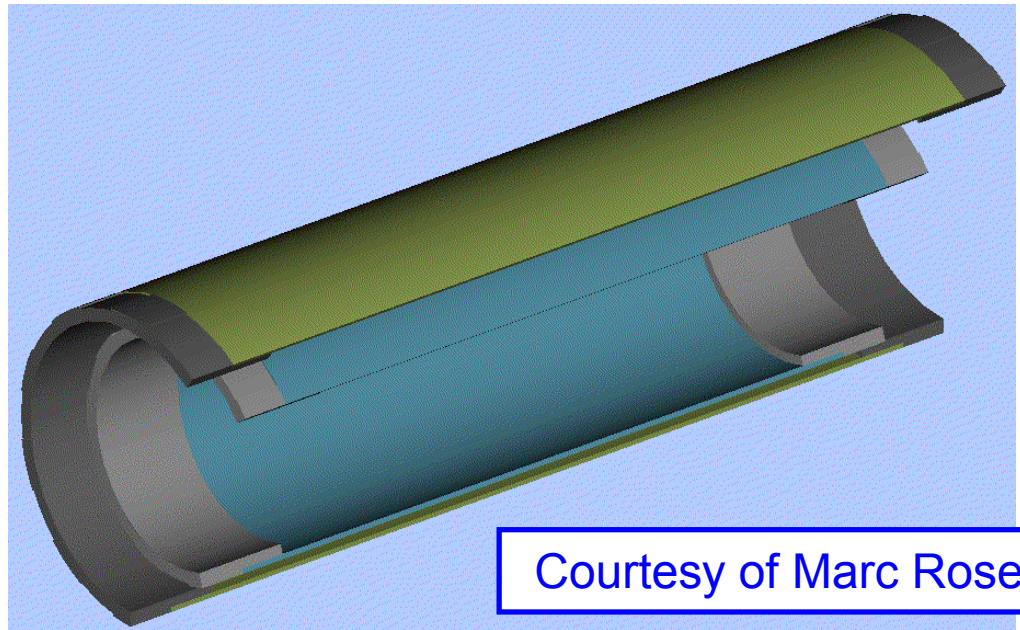
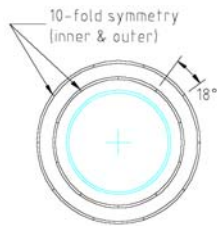
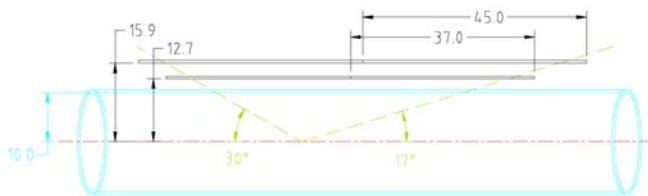


Detector Layout Concept

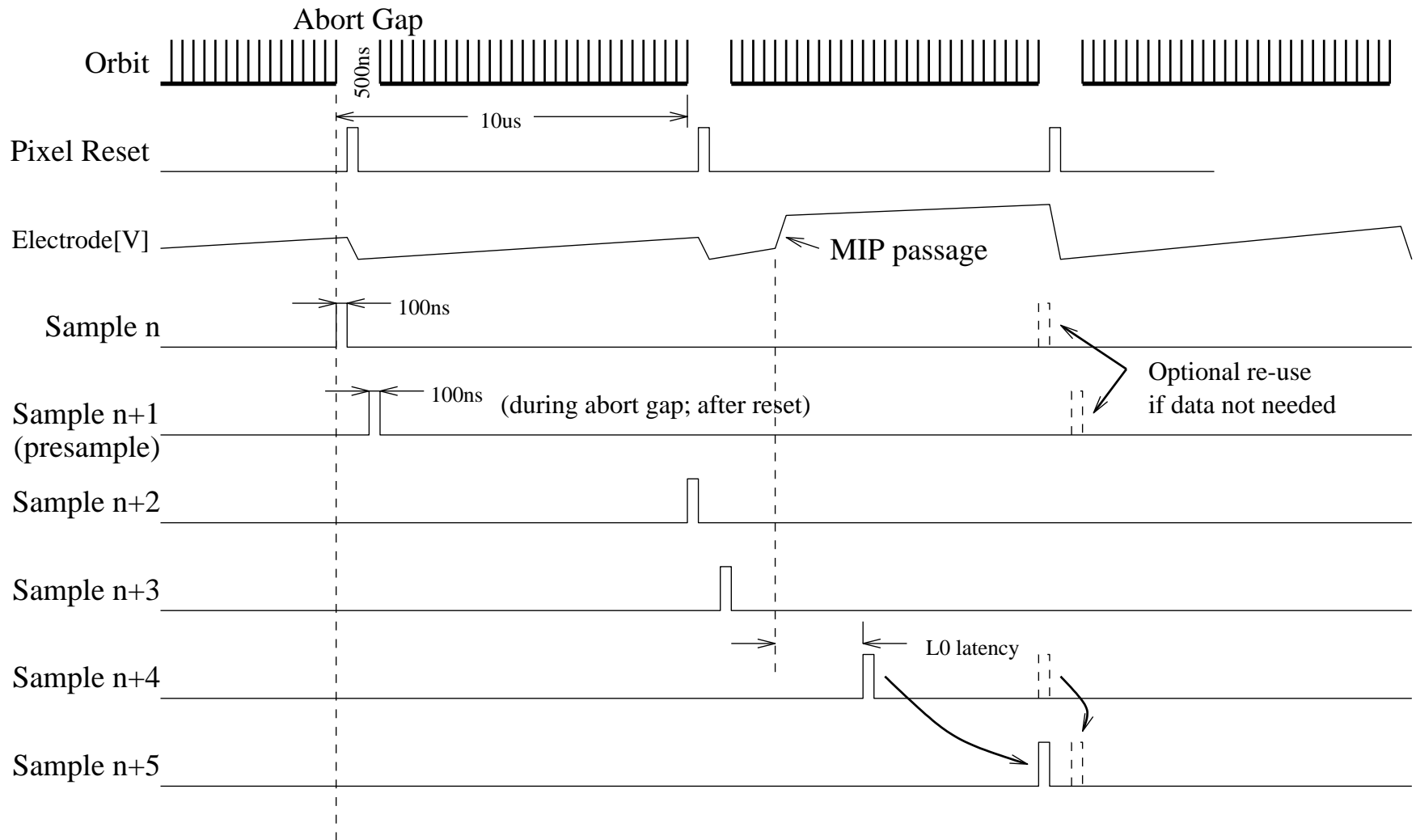
pixel-ladder concept



Significant Design Issues
But starting



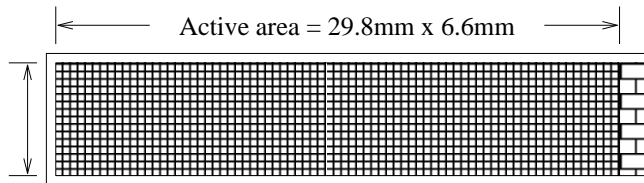
One Operating Mode



Event size

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155k Pixels

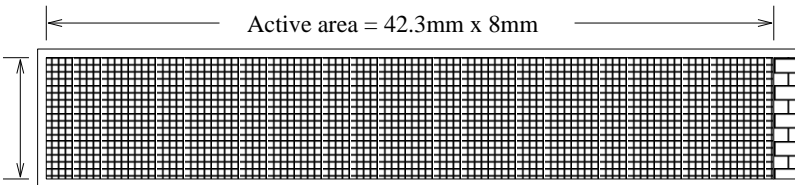
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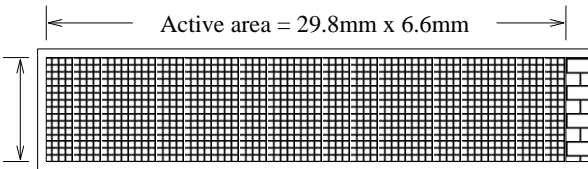
- Conservatively take 1% as Occupancy



1880 x 356 = 669k channels

2 layers * 24 HL = 32M pixels

320k Pixels



1324 x 293 = 388k channels

2 layers * 20 HL = 15.5M pixels

155k Pixels

- 1 Byte/pixel (8bit ADC) sufficient
- **However**, need ~25 bits of address info
- 4 Bytes/pixel → 620-1280kB/event
- Can reduce with clustering/track matching?



Required Transfer Rates

- CAP1 architecture (if $10\mu\text{s}$ max. latency):

- 15mm radius:

- 67 Gpixels/s
- $\sim 1\text{Gpixel/s/pin}$

- 10mm radius

- 39 Gpixels/s
- $\sim 0.5\text{Gpixel/s/pin}$

Two ways around:
- Multi-orbit
- "Tiling"

- CAP2 architecture ($\geq 100\mu\text{s}$ max. latency):

- 15mm radius:

- 6.7 Gpixels/s
- $\sim 100\text{Mpixel/s/pin}$

- 10mm radius

- 3.9 Gpixels/s
- $\sim 50\text{Mpixel/s/pin}$

Real max. latency
Set by $\langle L1/L2 \rangle$ rate



The Bottleneck

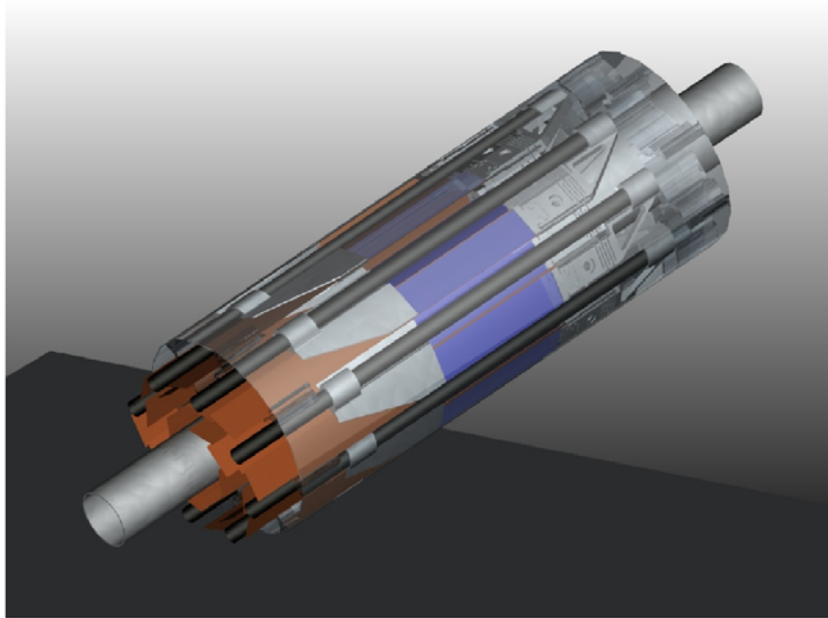
- Not trivial, but probably possible to:
 - Sample with adequate SNR
 - Read data off pixel with small enough latency
 - Provide periodic analog resets without incurring deadtime
- However:
 - Not easy to get this torrent to the electronics hut
 - Exploring 2 different fiber optics schemes
 - Custom SiGe mixer/modulator may be a solution
- Looks like can fit everything in one COPPER crate:
 - 1 high-speed fiber/half ladder
 - 1 high-speed fiber/FINESSE
 - Each FINESSE does all CDS/offset calculations
 - CPU does clustering?



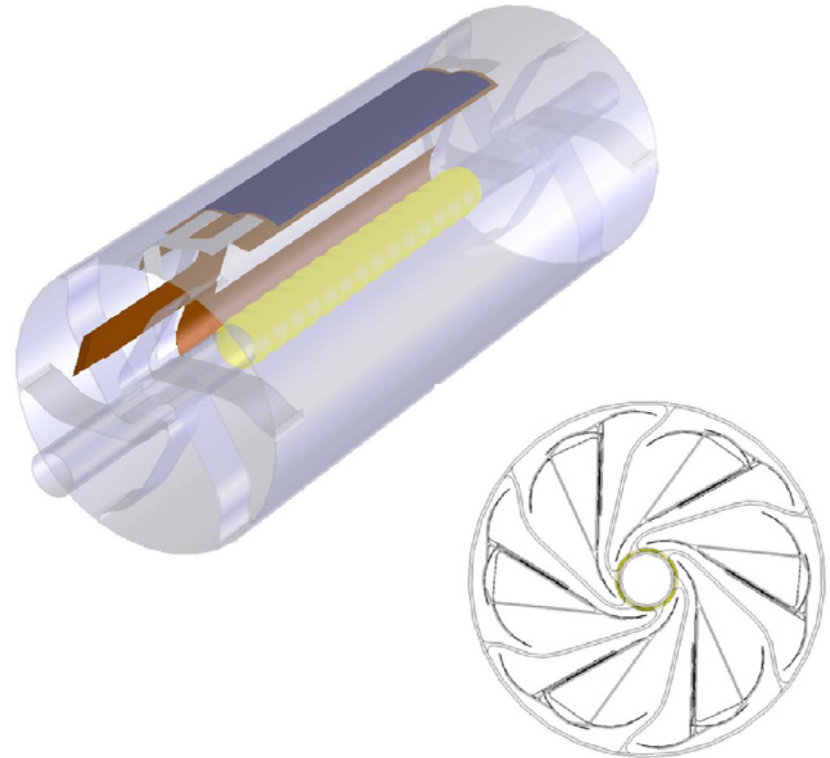
Mechanics

Very preliminary

Mechanical concepts of STAR Micro vertex upgrade using ultra-thin CMOS MAPS *



Tension concept



Self supporting Venetian blade concept

* Curtsey to Howard Wieman, LBL, STAR group

