Belle Monolithic Thin Pixel Upgrade – Testing Update

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On Behalf of the Monolithic Pixel Gang
Belle General Meeting
March 2004

Motivation

- Upgrade Advocacy (March 1997 Varner & Sahu)
  - Simplistic evaluation of the raw contributions to vertexing
  - Argued for improvement

Belle Note # 226

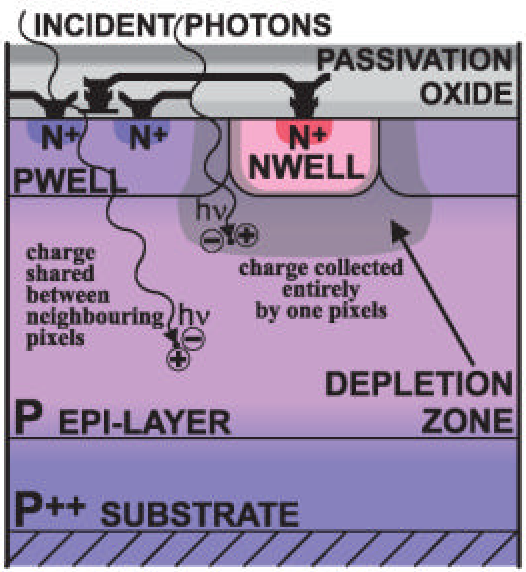
- Now update with experience of excellent KEKB performance
  - Occupancy
    - * At 20x background, even with segmentation ("striplet" option) and shorter shaping/pipelined readout – a concern
  - Improvement
    - Have been discussing in context of a x2 improvement, striplet option is probably a draw
    - One of the few areas in which the detector can be improved to exploit Super B statistics

Momentum Toward APS upgrade

- Globally, there has been much Active Pixel Sensor progress recently:
  - LEPSI/TESLA(MIMOSA) & LBNL/STAR prototypes
    - Hawaii has evaluated STAR prototype
    - RAL (APV25) also getting into the act
  - Hawaii has fabricated 2 B-factory prototypes (CAP1,CAP2)
    - Will explain more about/first test data today
  - Beam test of Belle pixel prototypes in the next few months
  - There has been R&D into using hybrid pixels
    - Choice for LHC
    - Simulation results show limited benefit – too thick, too large
  - In the spirit of "adiabatic" improvements, we may not have to wait for a "Super B shutdown", can replace SVD inner layer with pixels
    - <u>Comparatively low cost, most hard work done by industry</u>

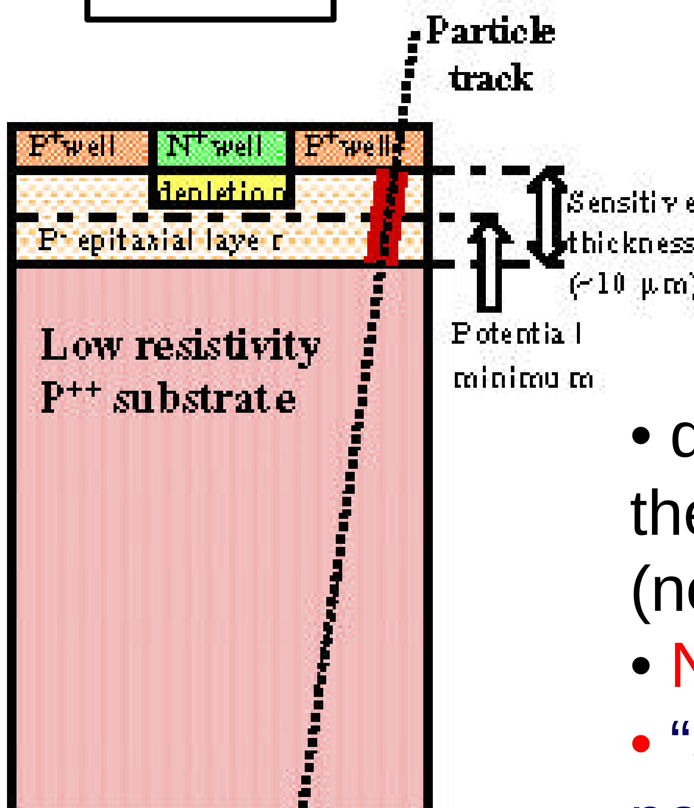
Basic Technology: Standard CMOS

CMOS Camera



Because of large Capacitance, need Thick DSSDs
-- APS can be VERY Thin

Particle Detector



Standard CMOS:

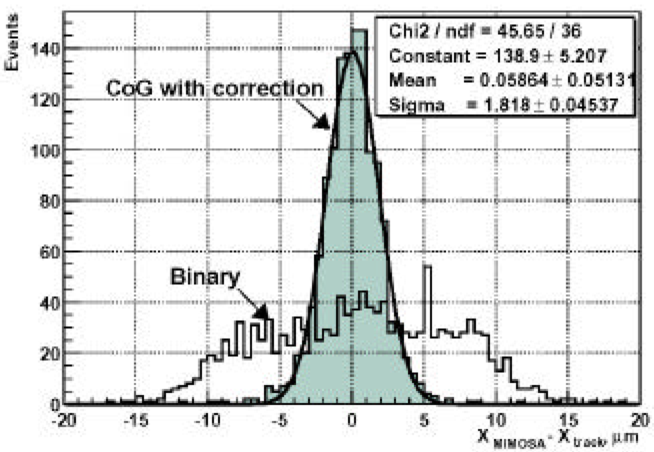
- Low Power
- Excellent Transistors
- Tight Process Control
- Excellent Uniformity
- High volume, low cost
- Large ADC, DSP base

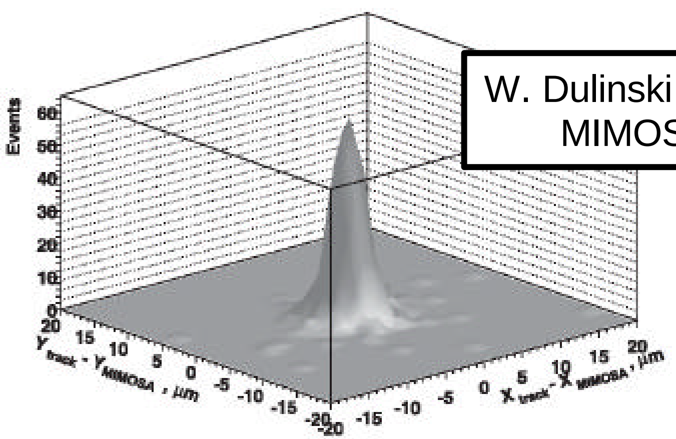
Key Features:

- q collection via thermal diffusion (no HV)
- NO bump bonding
- "System on Chip" possible

Promising Results Reported

CMOS MAPS particle tracking performance (20 μm pitch)





W. Dulinski [LEPSI]
MIMOSA4

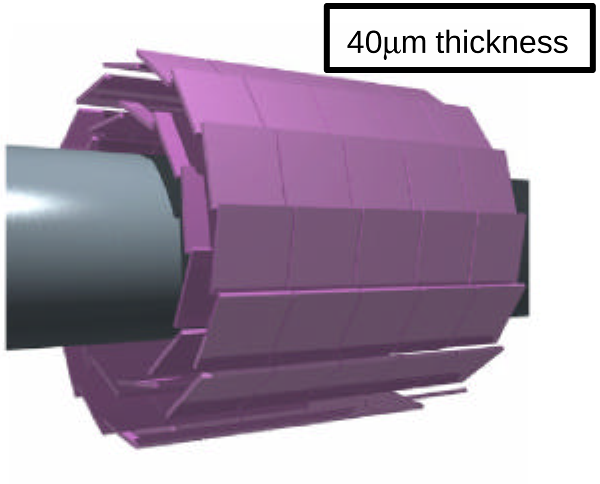
ENC ~10 electrons: S/N>30
Efficiency (5σ seed cut): $\varepsilon_{MIP} > 99\%$
Spatial resolution: $\sigma = 1.4$ μm

Demonstrated on several devices in various submicron CMOS processes:

AMS 0.6 μm, 14 μm epi
Alcatel 0.35 μm, 4 μm api
AMS 0.35 μm, no(!) epi
…
TSMC 0.25 μm, 8 μm epi
(LBL team)

+UH, RAL

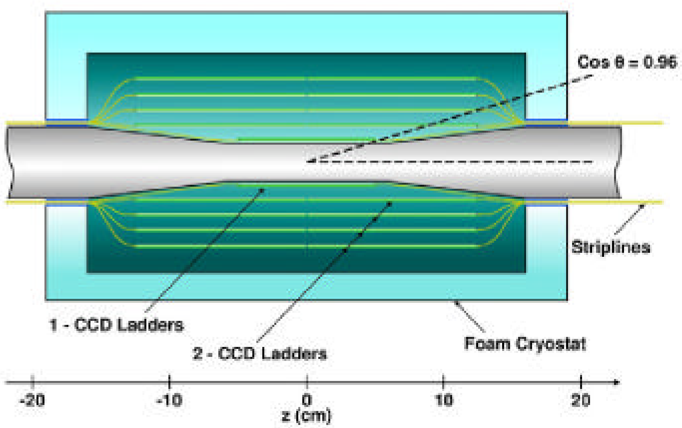
Other Experiments Considering



STAR μvertex detector

1. First upgrade (x4 present luminosity, 2006):
   10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008):
   2 – 5 ms readout (integration) time

Super-Belle: 10μs ?



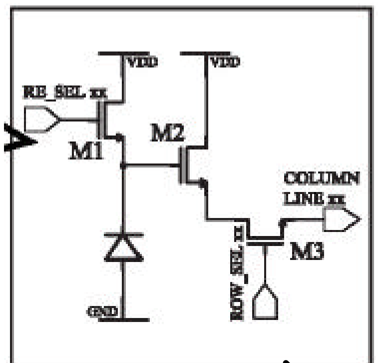
TESLA Vertex Detector*

1. Outer layers readout time: 100 -200 μs
2. Innermost layer readout time: 25 -50 μs

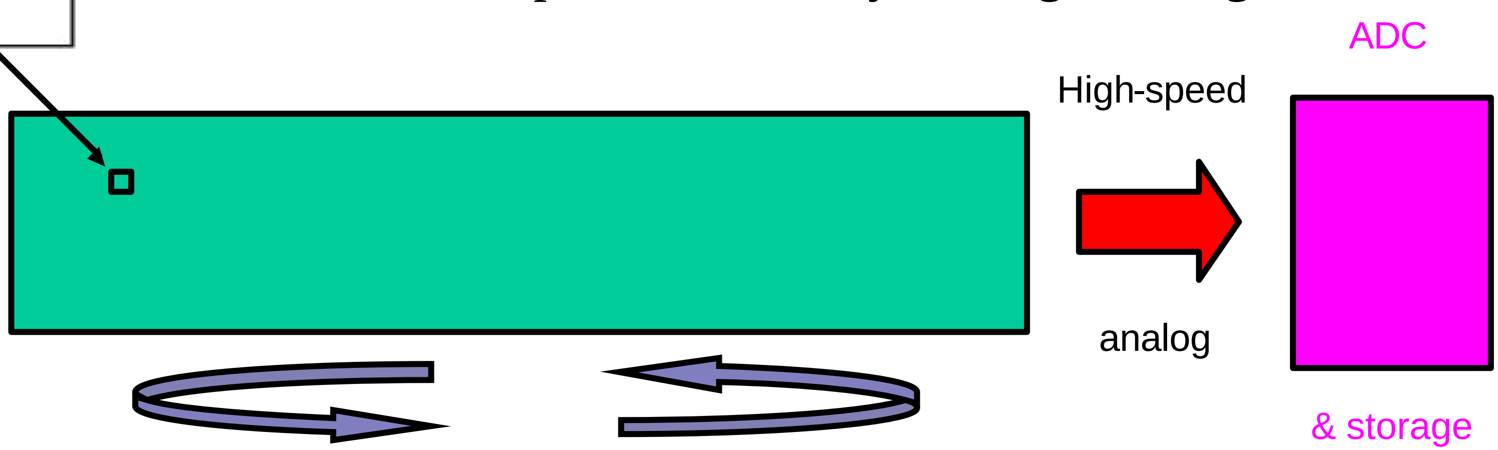
*NLC/JLC: t~10 ms

Continuous Acquisition Pixel (CAP)

- Conceptually Simple
  - Analog reset, take sample frame and then difference
  - Continuous “Correlated Double Sampling”
  - Row-wise analog shift out as fast as possible:
    - Consider 22.5μm square pixels
    - A few μm resolution possible for good SNR
    - Readout speed limited by analog settling



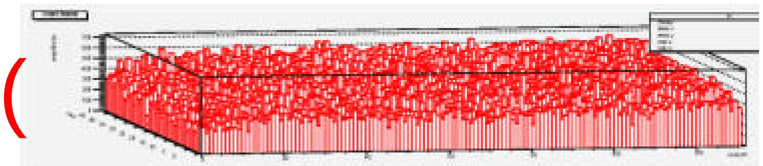
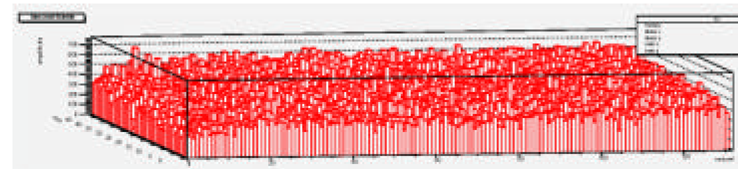
Standard APS pixel



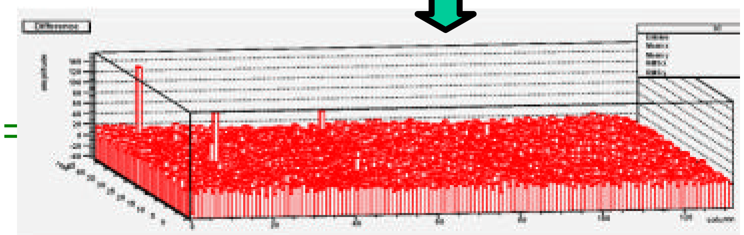
Pixel Array: Column select – ganged row read

Low power – only significant draw at readout edge

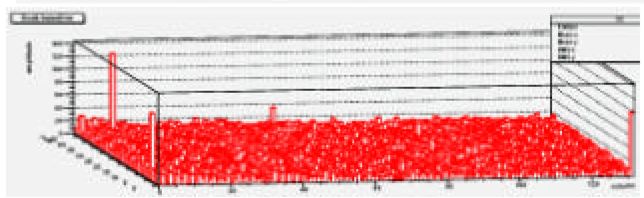
CAP CDS

( - )

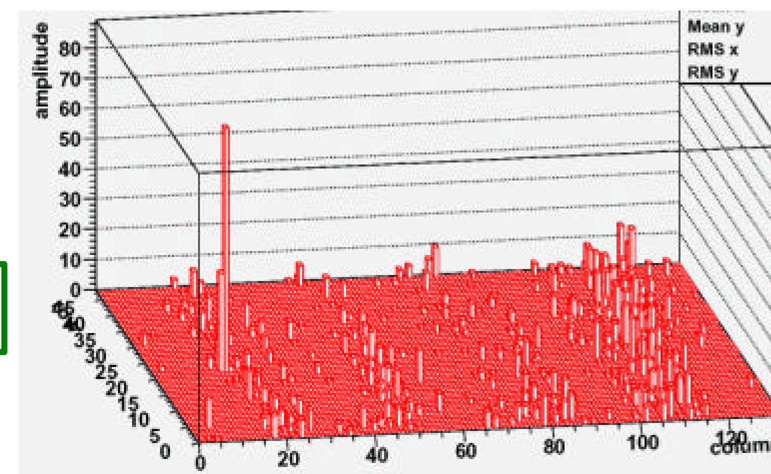
Frame 1 - Frame 2 =



- Leakage current Correction



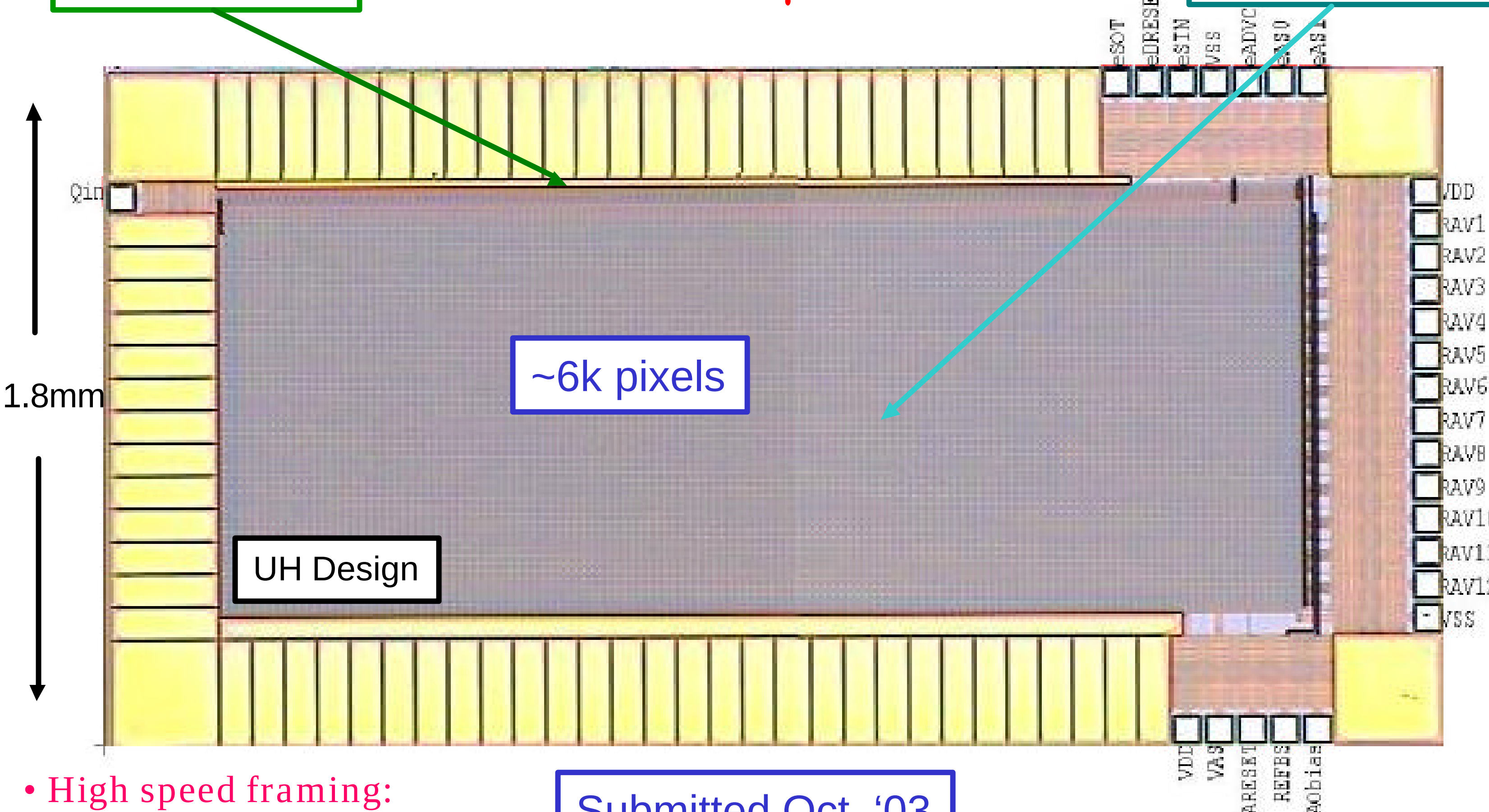
Naturally Masks “hot” pixels



Hit candidate!

CAP1 Prototype

- TSMC 0.35μm Process

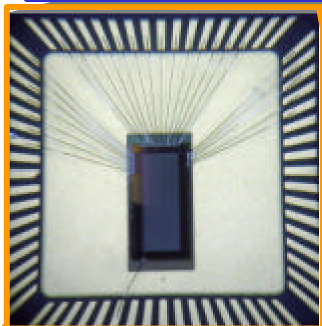


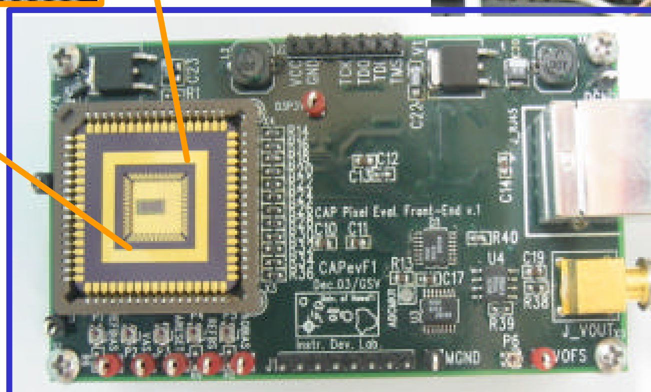
- High speed framing:
  - Target 10μs latency

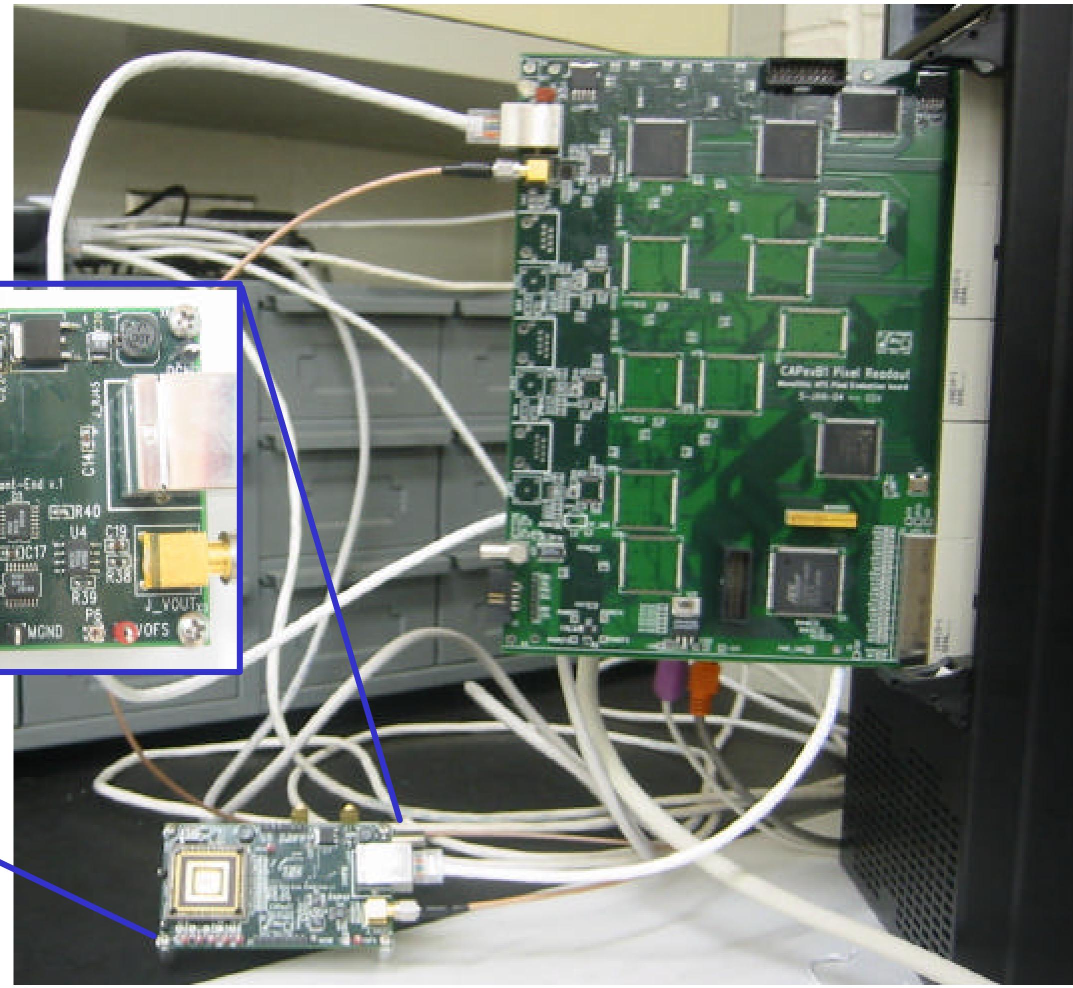
Submitted Oct. '03
Received early '04

"slow" readout resolution ~ 2μm
At higher readout speeds?

Prototype Test Bench

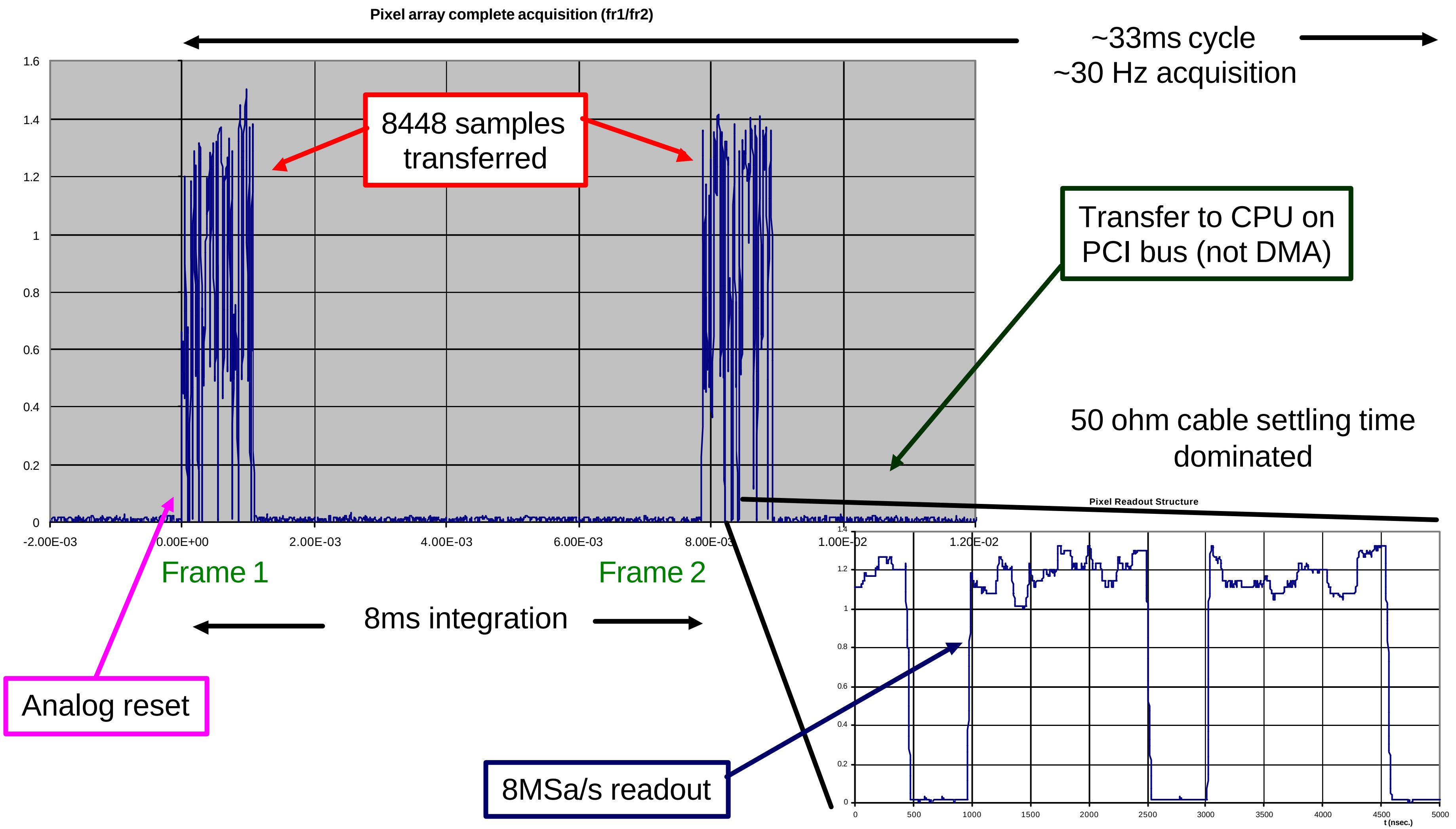




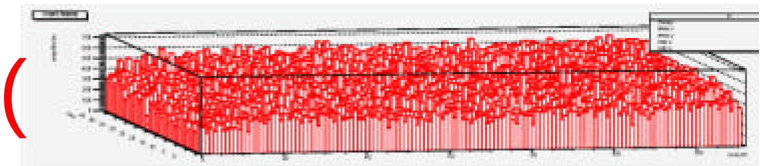
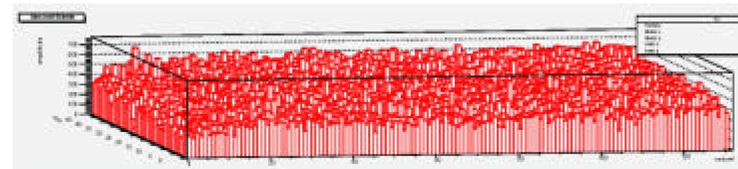


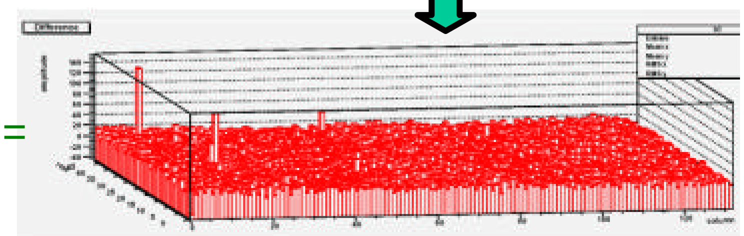
Compact PCI (cPCI) based

Cosmic Sampling Cycle

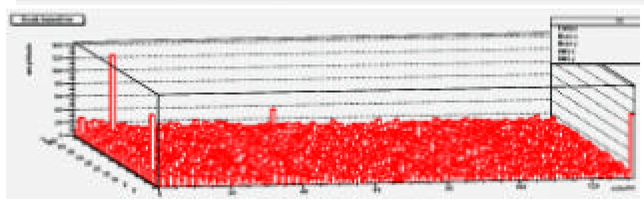


CAP CDS

( - )

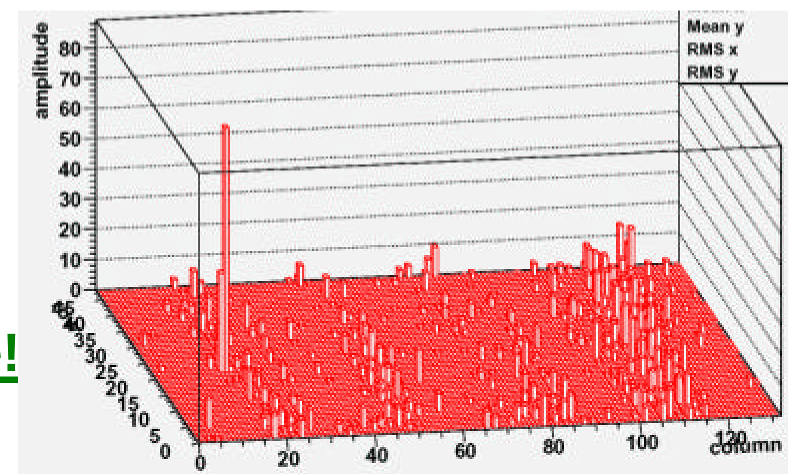
Frame 1 - Frame 2 = 

8ms integration

- Leakage current Correction 

Can readout/process
@ 30Hz – 25% livetime

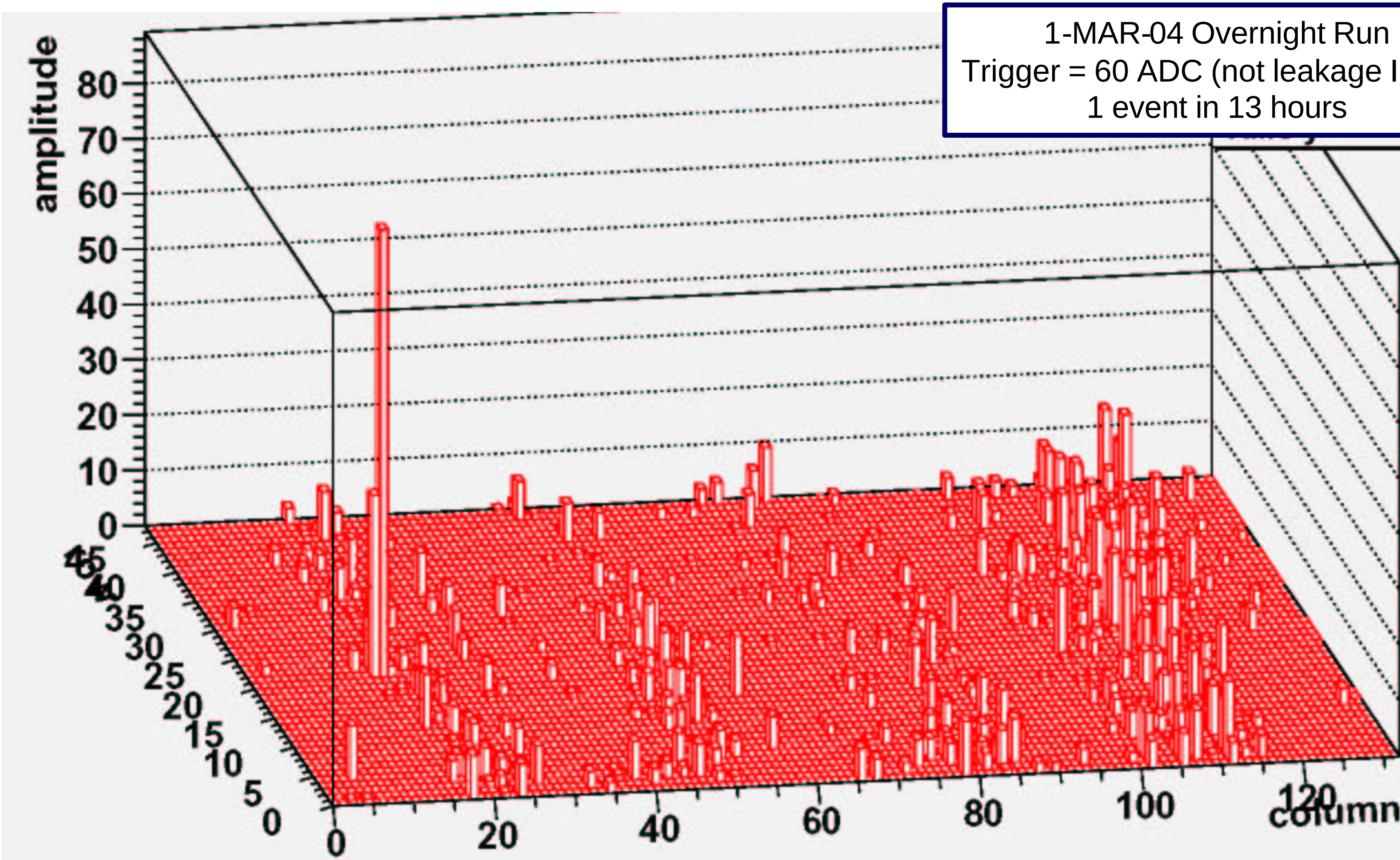
~fA leakage current (typ)
~18fA for hottest pixel shown



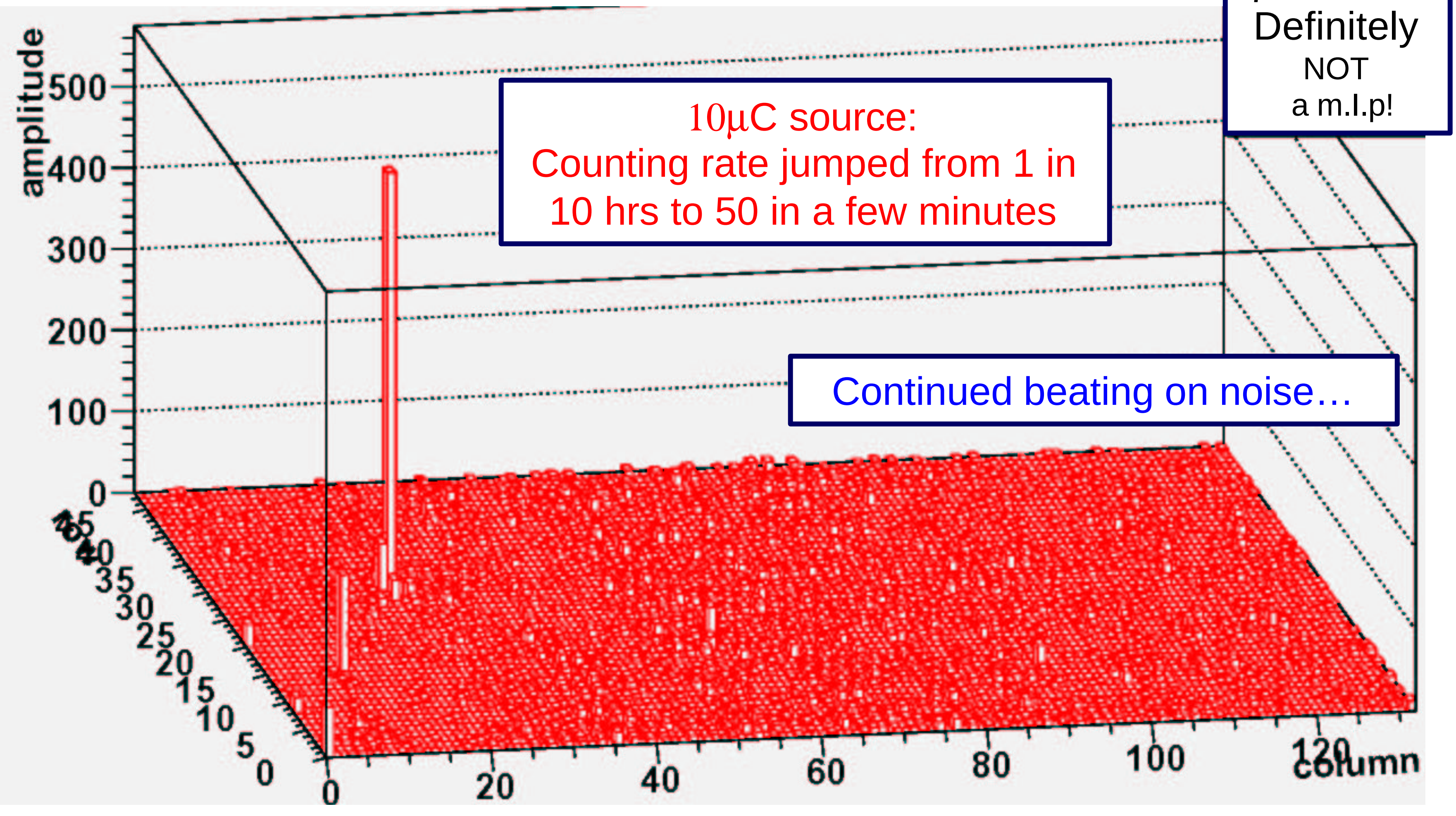
Cosmic muon candidate!

First Cosmic Event

1-MAR-04 Overnight Run
Trigger = 60 ADC (not leakage I subt)
1 event in 13 hours



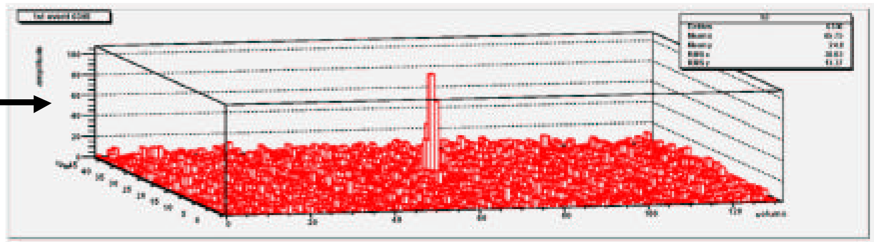
Source Check – Cs137

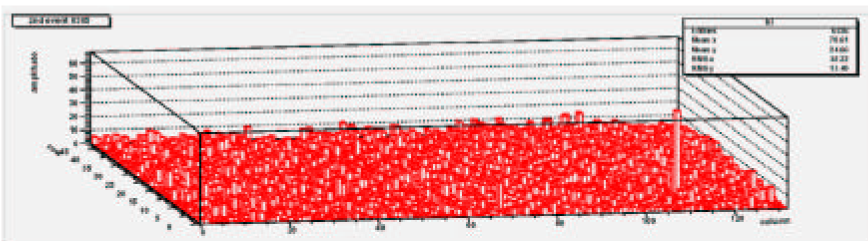


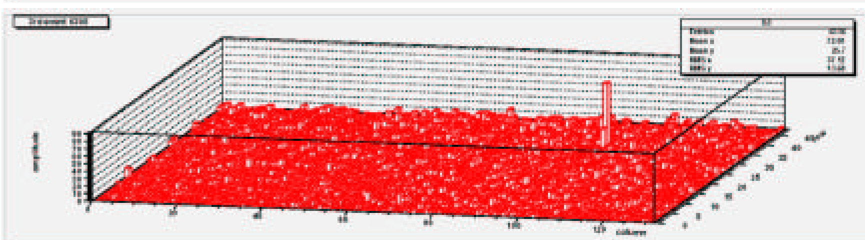
β- emitter
Definitely
NOT
a m.I.p!

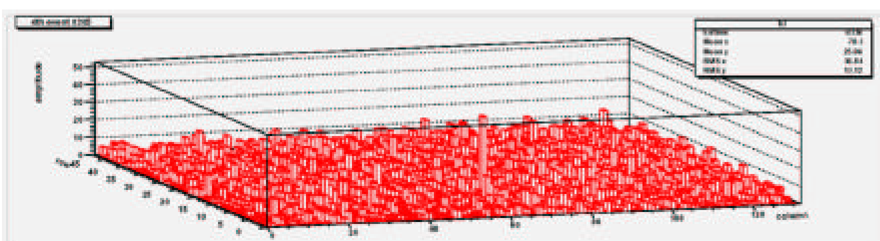
Continuing Cosmics

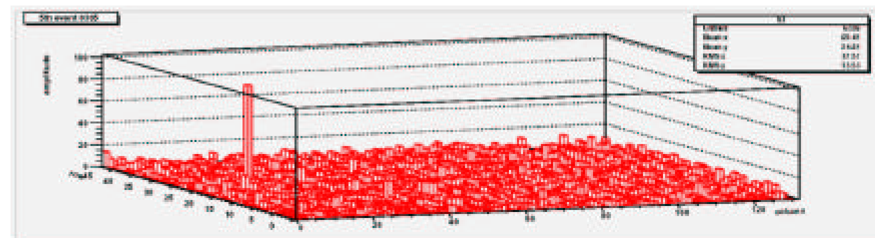
4-MAR-04 Overnight Run
Trigger = 45 ADC counts
7 events – much better noise

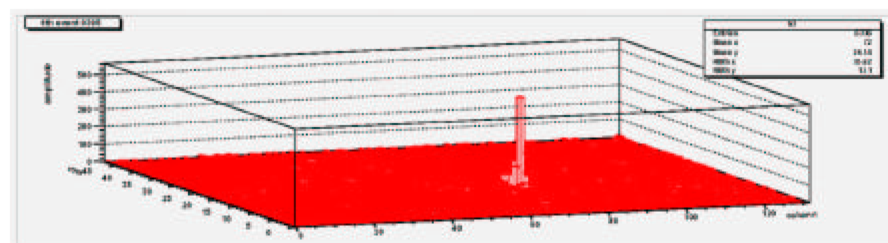


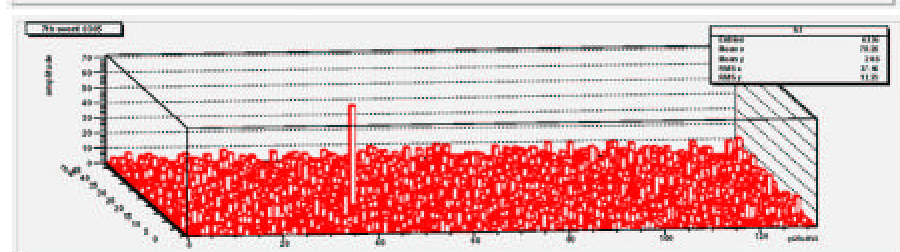




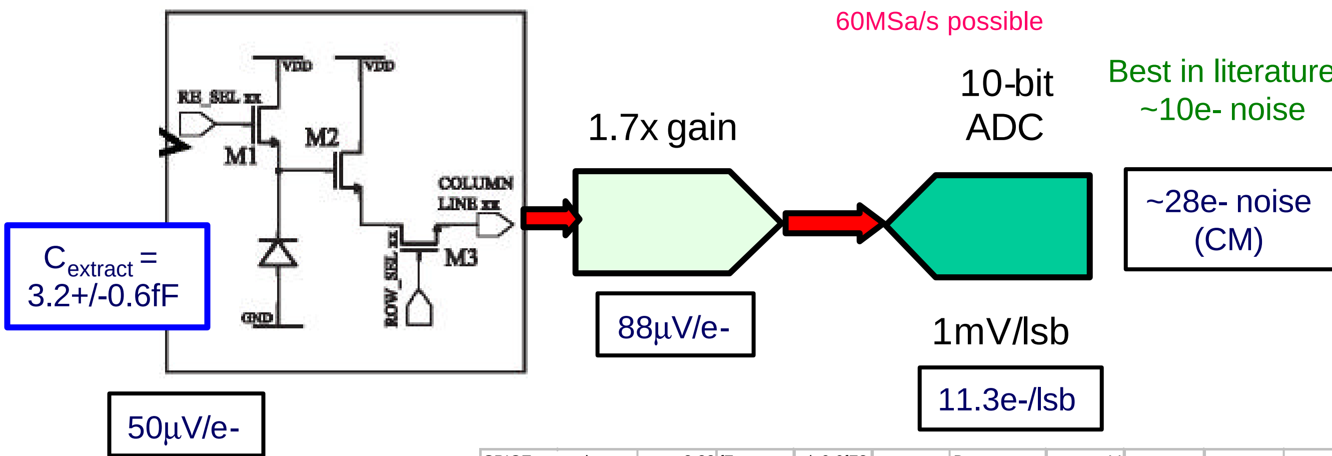








SNR Comparison



Even so, SNR ~ 20

Signal max. ~ 560e-

Assuming 50% Signal collection ε In Max channel

SPICE extraction:		3.22	fF	+/- 0.6fF?		Detector:	14	µm		
Q=	1.60E-19	C/e-	Q=C*V			DSSD ref:	300	µm	24000	e-hole pair/m.I.p.
V=	4.97E-05	V/e-				Geom SF:	0.046667			
chip transfer: (SPICE)		0.78	Vout/Vin			Signal:	1120	e-	max produced	
						Collection efficiency	0.5	w.a.g. -- in max channel		
Resistive Divider:		1	was 2:1							
CAPevF1 amp:		7	gain			Peak signal:	560	e-		
50 ohm series term:		0.5	voltage divide							
CAPevB1 amp:		0.65	gain							
Net transfer gain:		**1.7745**								
Sensitivity:		0.088174	mV/e-			**Expected SNR:**		19.75096		
CAPevB1 noise:		**2.5**	**ADC lsb noise**			**Sigma Set:**	7			
CAPevB1 ADC:		1	mV/lsb			**Threshold:**	60			
CAPevB1 sensitivity:		11.34122	e-/lsb			**m.I.p exp.**	49.37739			
CAPevB1 floor:		28.35306	e-							

Critical R&D Items

1. Readout Speed
2. Radiation Hardness
3. Thin Detector
4. Full-sized detector

1) High Speed Sampling

- CAP1 type architecture difficulties:
  - Significant strain on analog output transfer:
    - <<10ns settling time difficult

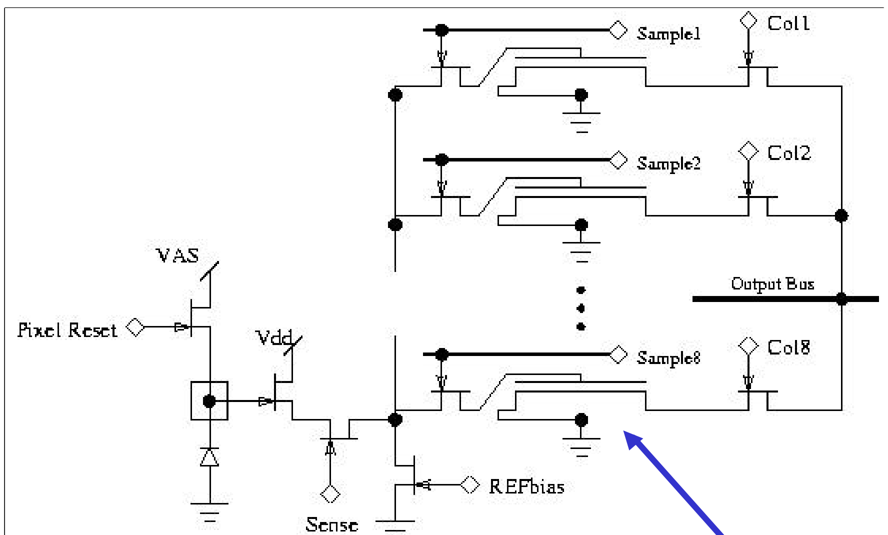
      (testing shows can work @ few kHz, but not @ 100 kHz)
  - Data volume reduction
    - Better if can provide true on-detector pipelining
    - Reduce power if constrict data flow to L1/L2 accepted events (100kHz→ 10kHz or 1kHz):

      40GSa/s → 4GSa/s or 400MSa/s

Possible to put a small pipeline in each pixel?

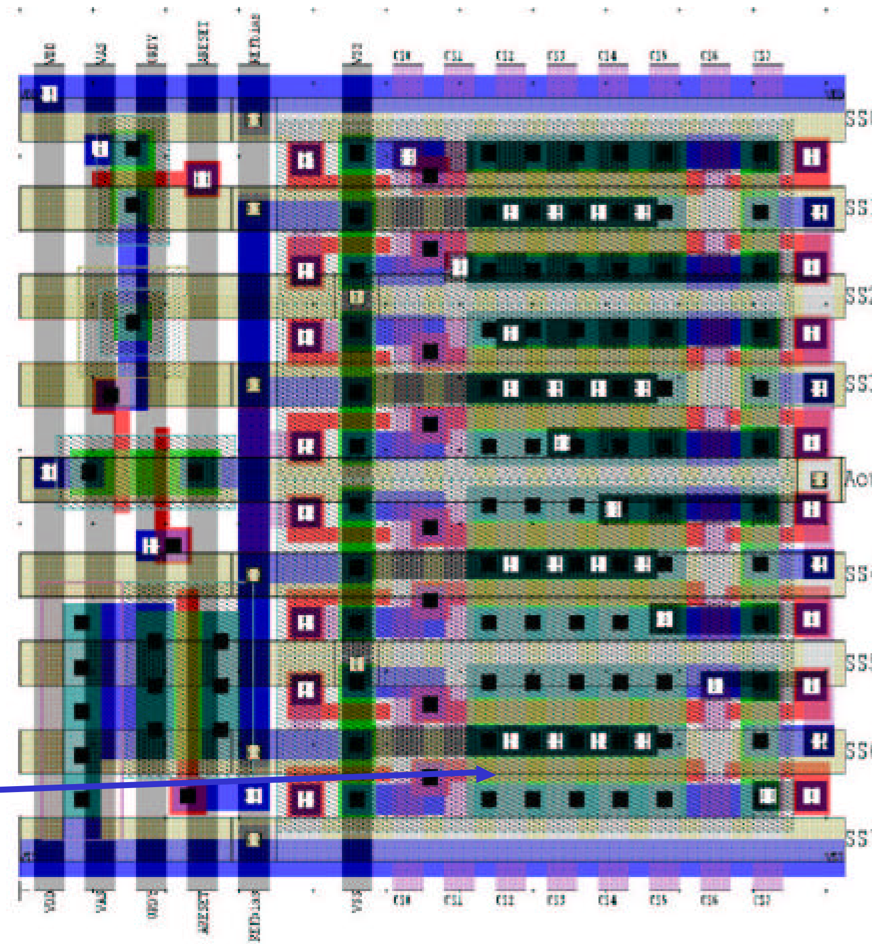
Octal-pipeline (in 22.5μm^2 pixel)

Yes!
Random access, decoupled
Read/Write



Storage cell

- 0.35μm Process 8x, more possible

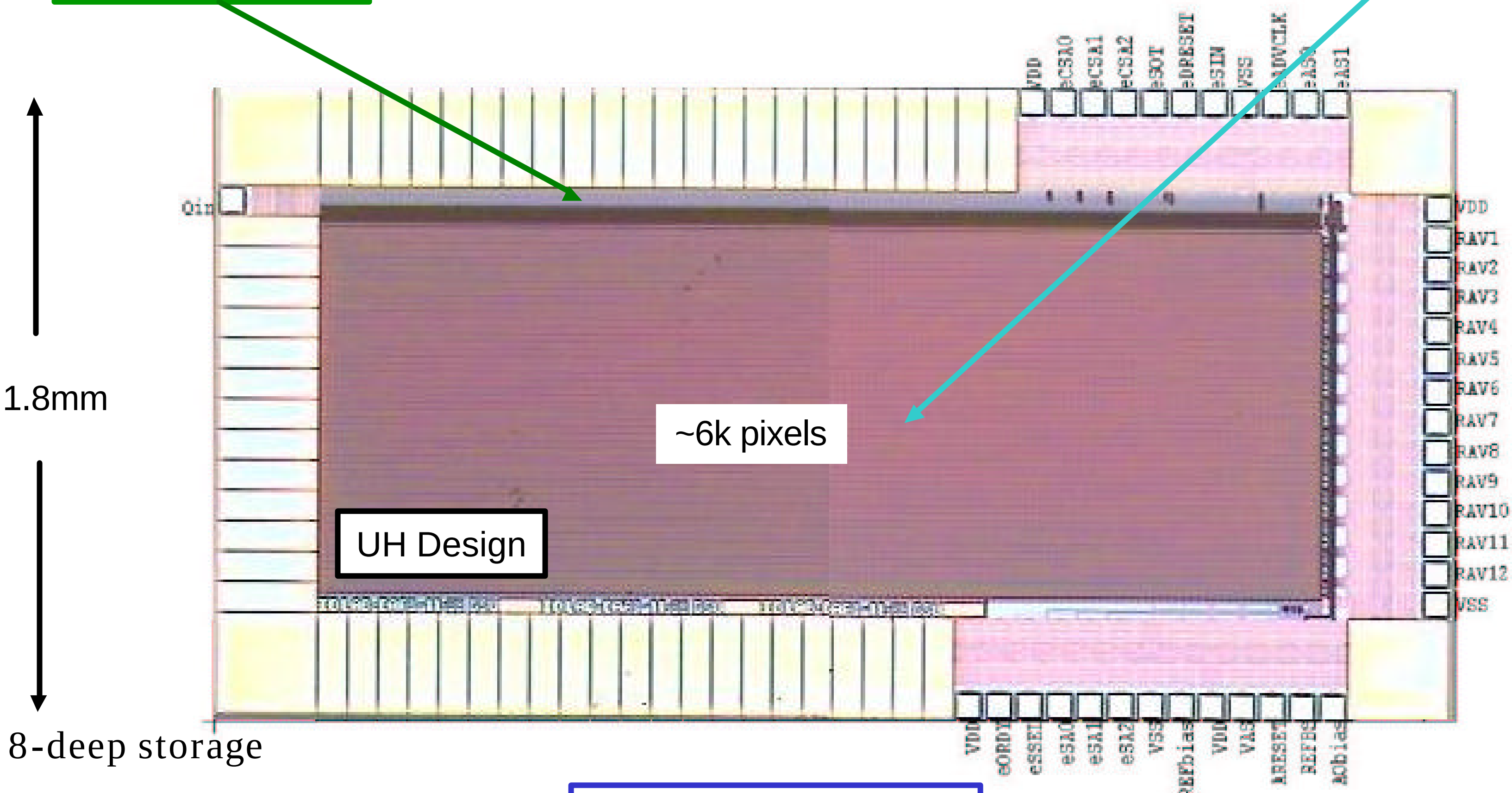


CAP2 Prototype

Column Ctrl Logic

• TSMC 0.35μm Process

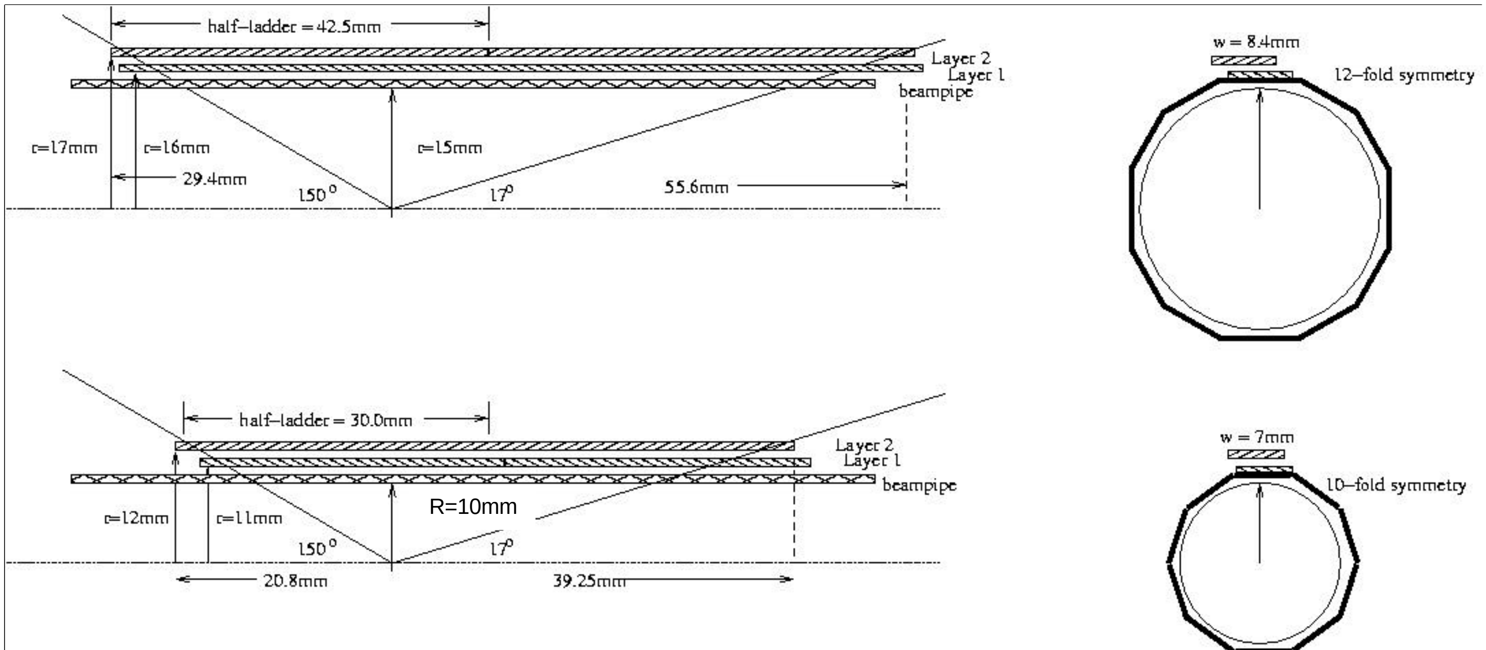
132x48 (22.5μm² pixels)



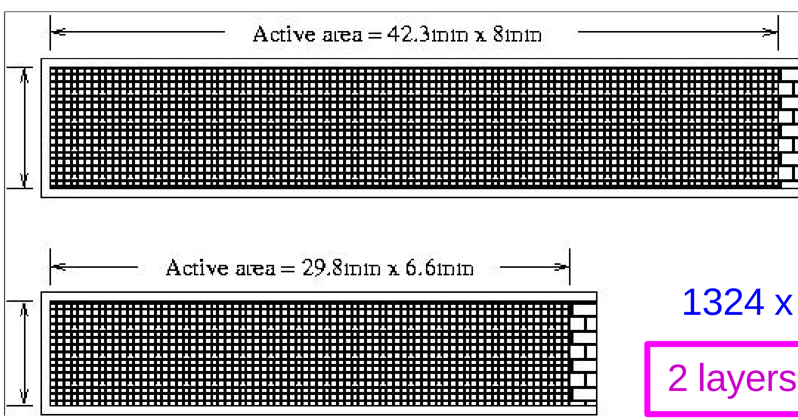
- 8-deep storage
  - Target 50μs latency
- Triggered readout

Submitted Nov '03
Start Testing Soon

Straw-Man Channel Count



Half-ladders:



1880 x 356 = 669k channels

2 layers * 24 HL = 32M pixels

1324 x 293 = 388k channels

2 layers * 20 HL = 15.5M pixels

Occupancy Scaling

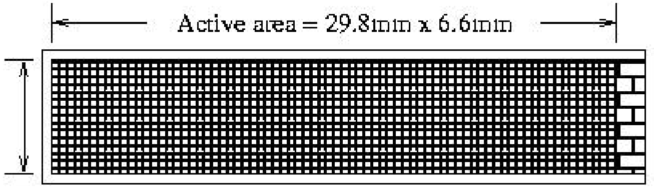
- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm^2
  - Pixel spatial reduction:
    - Pixel area = 22.5μm x 22.5μm = 506 μm^2
    - Reduction factor ~8400
    - Low E γ, reduced cross-section (~3% active thickness)
  - Pixel temporal loss:
    - 1.0μs SVD vs. 10μs PVD (could be improved)
    - Increase factor ~ 10-20
  - Grand total:
    - 10% * 20 * 8400^{-1} * 20
    - Can expect ~ 0.5% occupancy

(estimate 3% Striplet case)

Event size

- Conservatively take 1% as Occupancy

R = 1cm case



1324 x 293 = 388k channels

155k Pixels

2 layers * 20 HL = 15.5M pixels

- 1 Byte/pixel (8bit ADC) sufficient
- However, need ~25 bits of address info
- 4 Bytes/pixel → 620kB/event
- Can reduce with clustering/track matching:

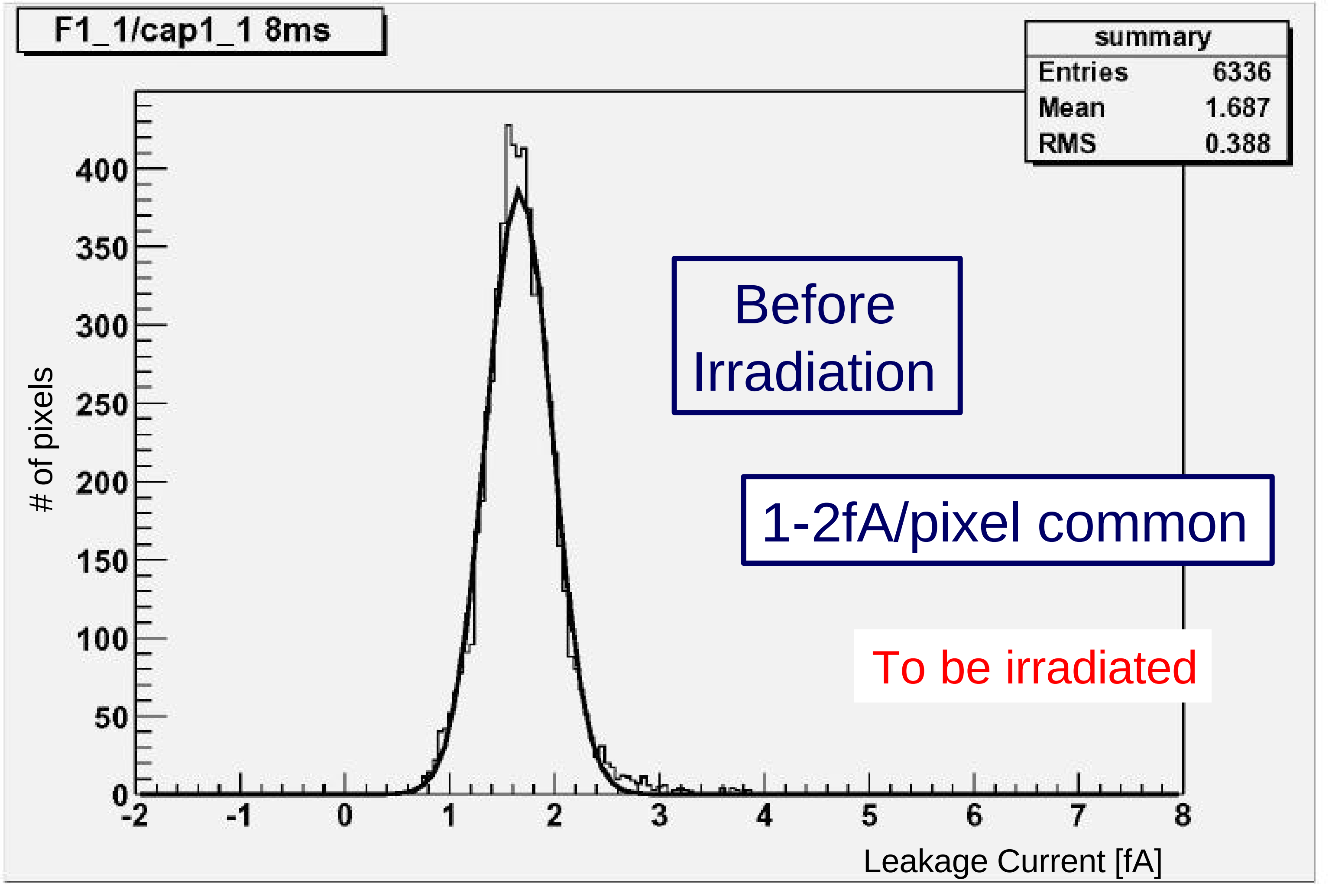
For instance, 1024 L2 trigger sectors → 16 unique tracks

~10kB/event

2) Radiation Damage

- As per the literature, the two problems of concern for use in a B-factory:
  - Leakage current increase
  - Charge collection loss (?) (~40%)

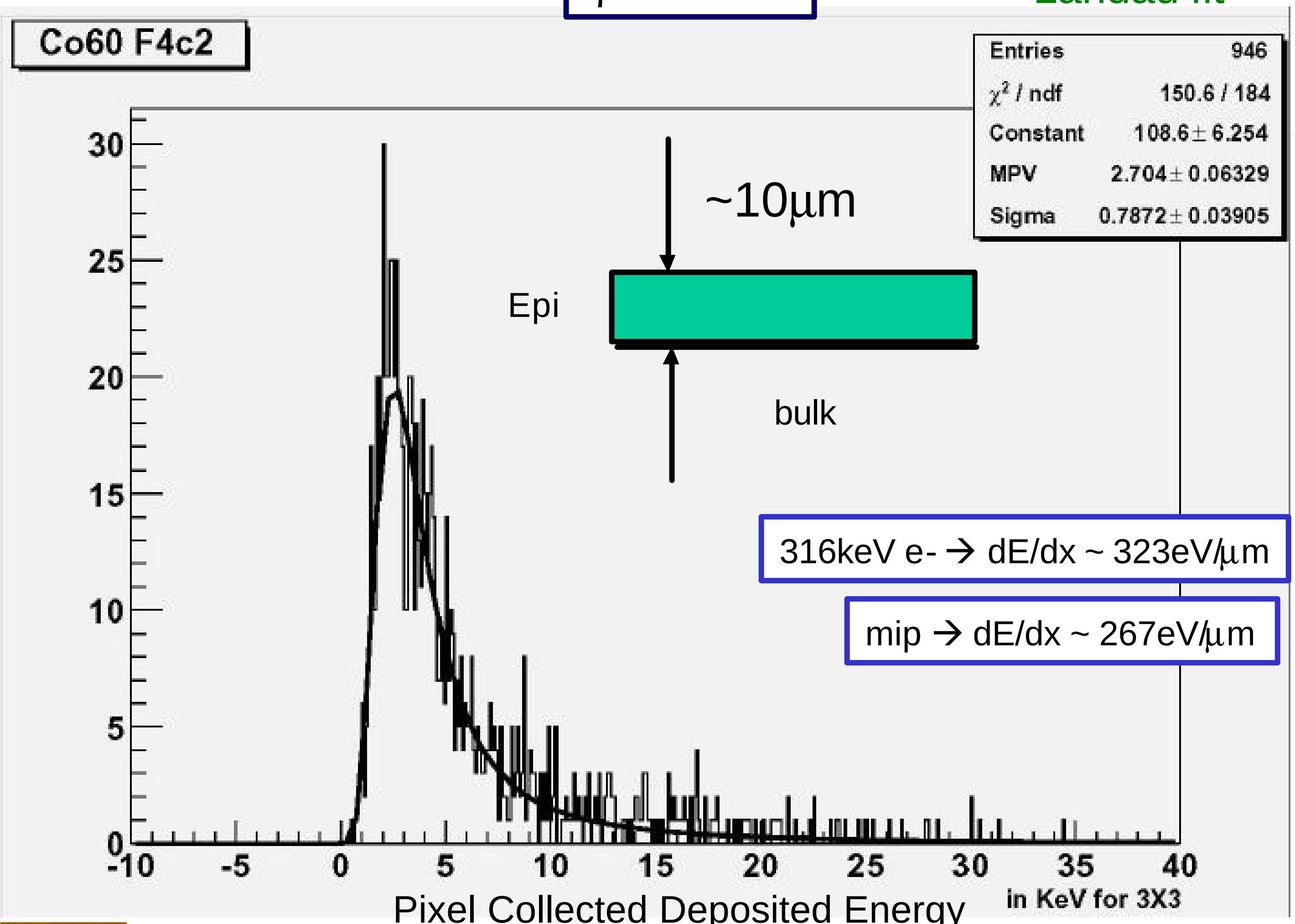
Leakage Current

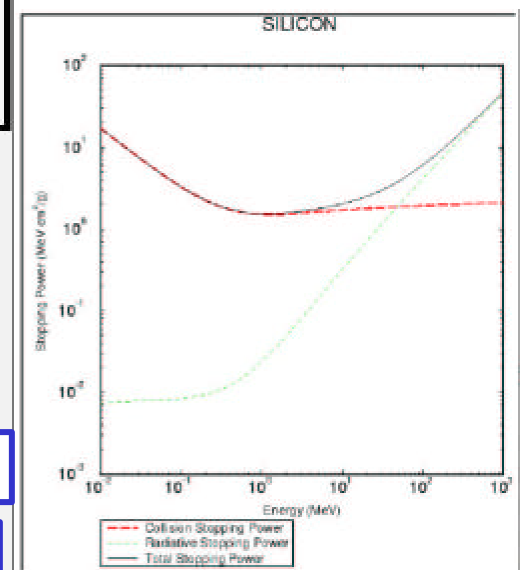


Charge Collection Efficiency

β- emitter

Landau fit



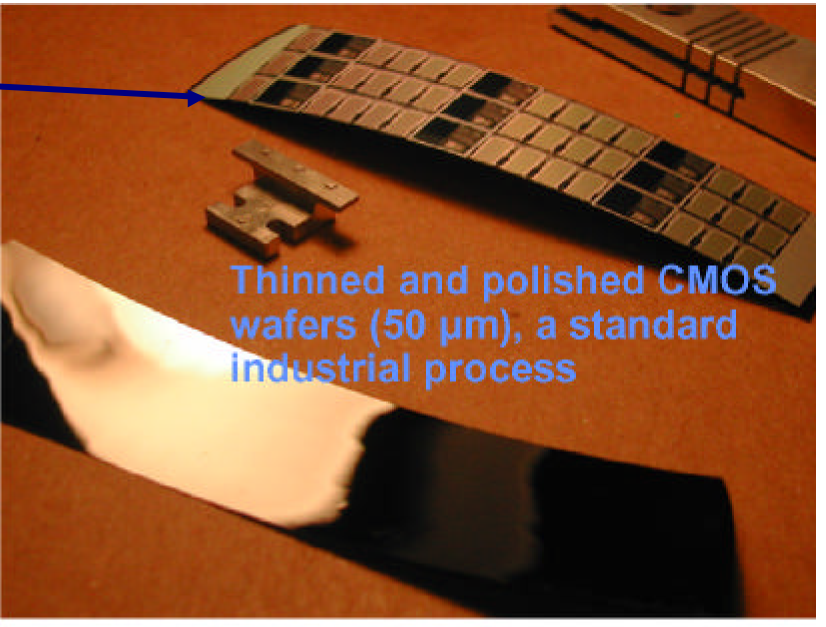


Will Check After Irradiation

3) Thin is In

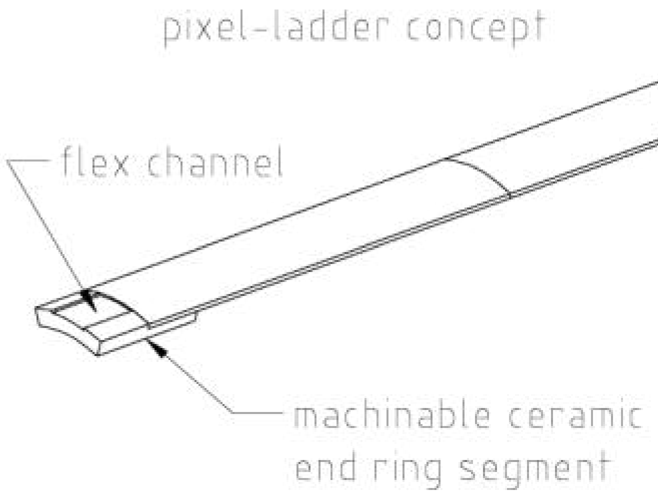
1. **Thinning the substrate to 50 µm (or less)**
2. **Low mass (air?) cooling: keeping down the power dissipation (~100 mW/cm²)**

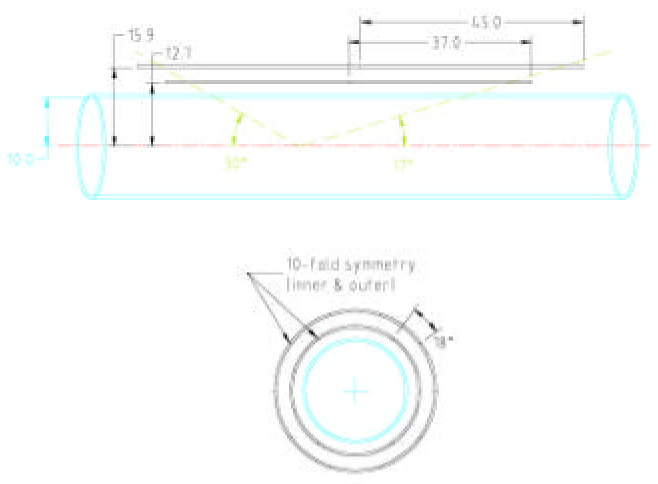
LBNL old wafer



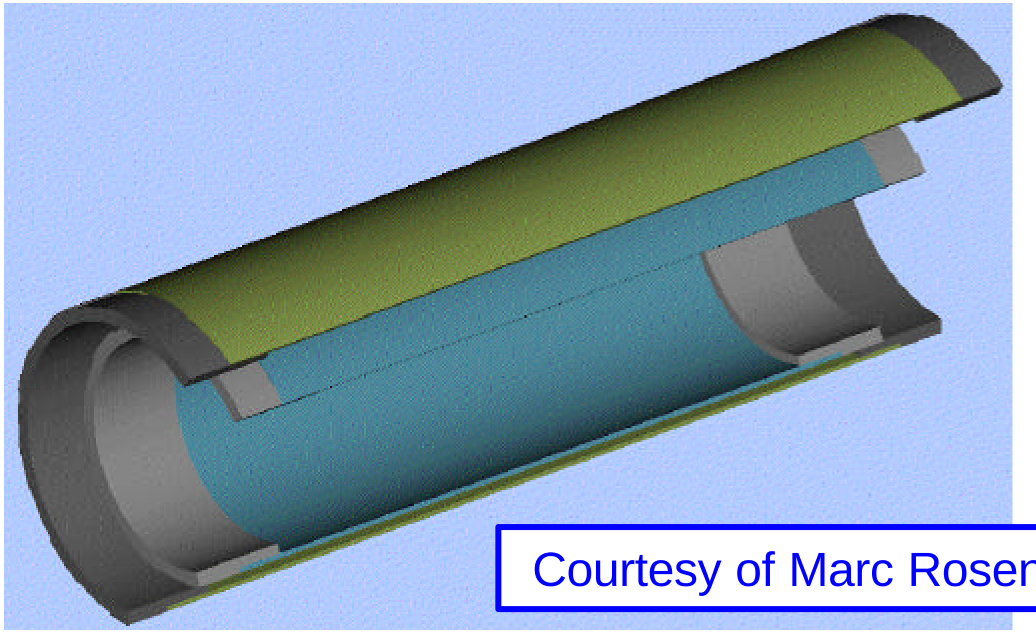
Starting to play with thin Samples @ UH

Detector Layout Concept



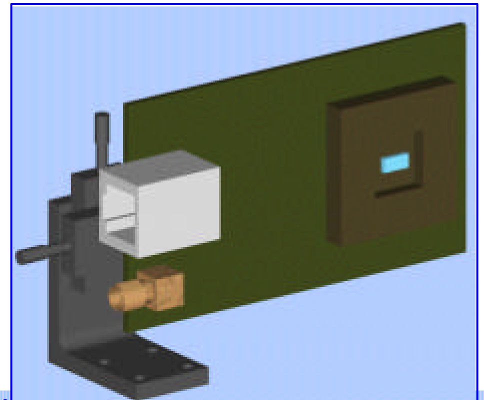


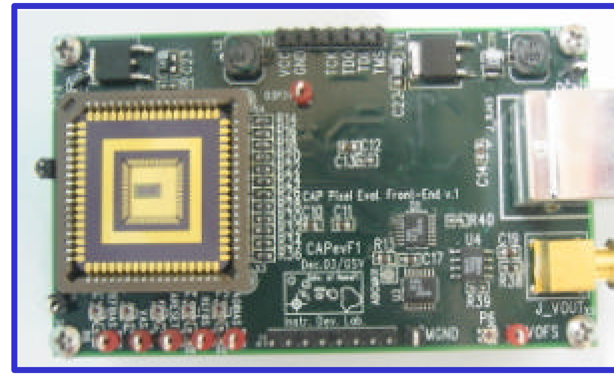
Significant Design Issues
But starting

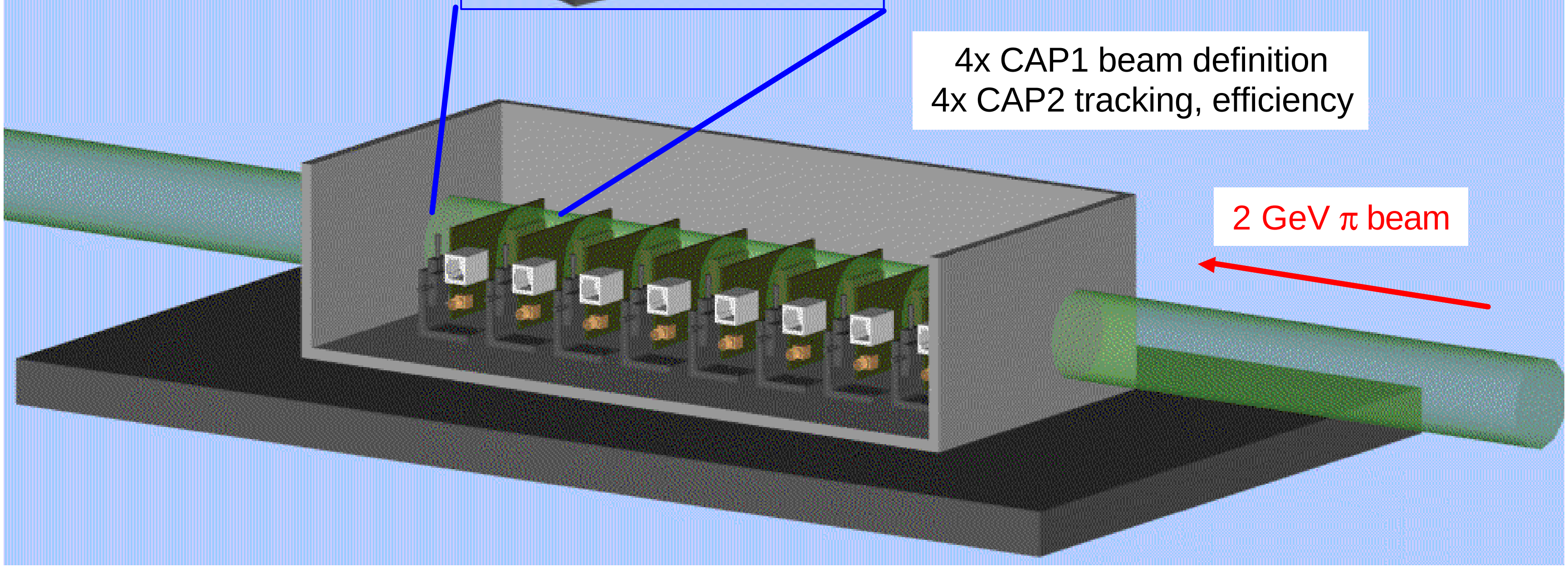


Courtesy of Marc Rosen

Beam Test Configuration







Critical R&D Items

Belle Note Soon!

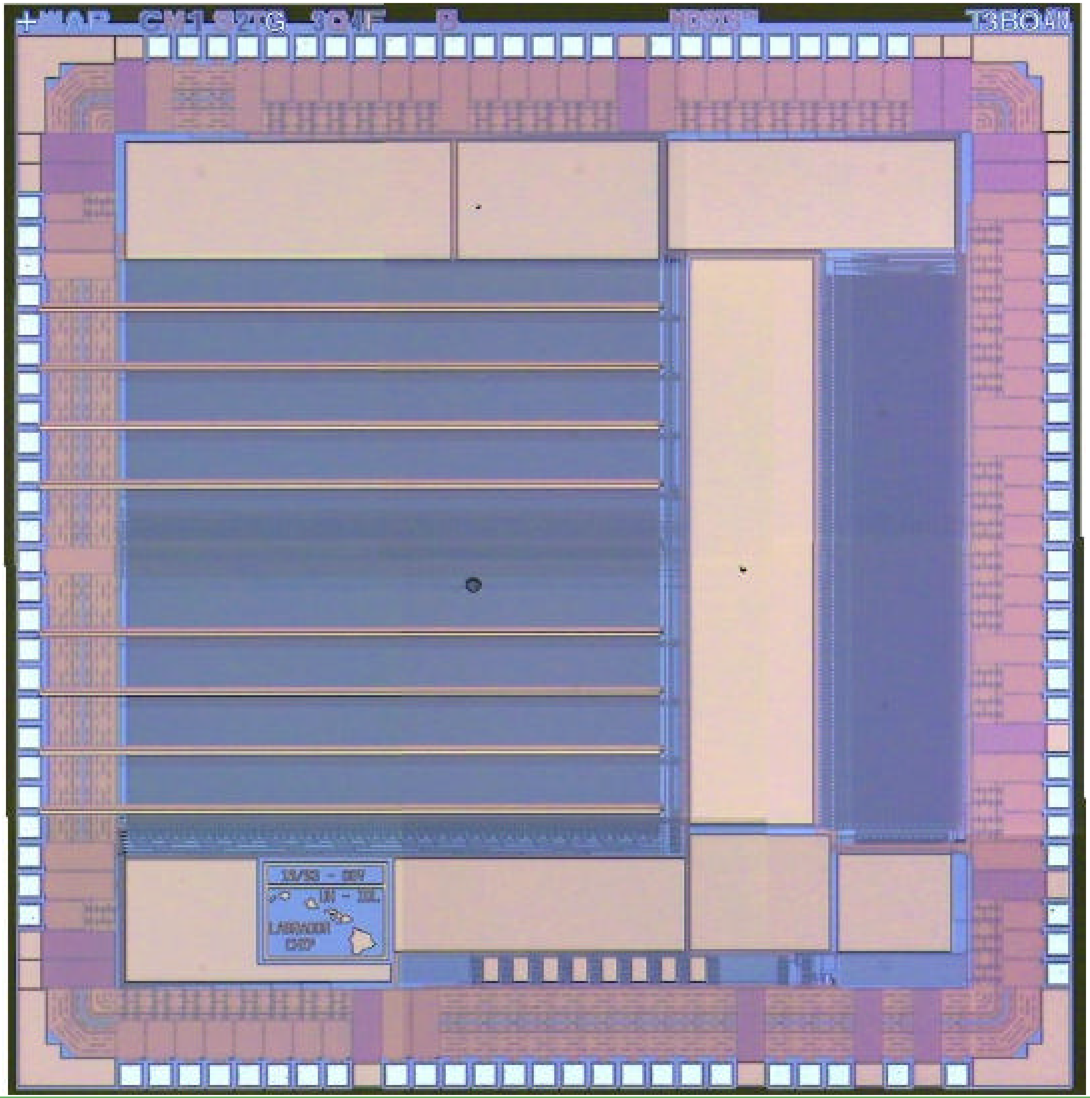
- Readout Speed:
  - Have demonstrated basic functionality
    - Crank up sampling/readout speed (CAP2)
    - Upgrade readout based upon lessons learned
- Radiation Hardness:
  - Have brought 3x detectors to Japan for irradiation
    - Quantify leakage current, charge collection loss
    - Short integration time helps!
- Thin Detector:
  - Plan to do a trial thinning @ Stanford CIS (C. Kenney)
    - Preferably on a full-sized detector
- Full-sized detector:
  - Ready to submit in summer, funding?

Summary

- Excellent Initial Results:
  - On track toward a beam test very soon
    - SNR optimization (~20:1)
    - Leakage current @ large irradiation (during BGM)
  - Much effort yet required:
    - Enormous data volumes/bandwidth requirement
    - Support, stability and cooling of thin detector – without adding significant mass
  - Large data reduction possible – Track matching?
  - Opportunities to participate
- Beam Test:
  - All welcome – please join
  - Based upon results – full-sized detector

No “showstoppers”, prototype qty enough to build PVD1.0

Back-up slides



CAP1 Concept

- Automatic CDS – always sampling
  - When receive L1 trigger:
    * sift data in sync pipe and provide the difference in value for orbit with trigger and preceding orbit
  - Analog reset
    - If reset once every 1oo orbits, 1% "deadtime"
    - 1μs "reset" and 10μs to obtain a baseline sample
    - Possibly even less, depending upon dynamic range and background
    - Can build "intelligence" into reset
    - Minimization of leakage current important
    - Relatively simple to fabricate

Required Transfer Rates

- CAP1 architecture (if 10μs max. latency):
  - 15mm radius:
    - 67 Gpixels/s
    - ~1Gpixel/s/pin
  - 10mm radius
    - 39 Gpixels/s
    - ~0.5Gpixel/s/pin
- CAP2 architecture (>= 100μs max. latency):
  - 15mm radius:
    - 6.7 Gpixels/s
    - ~100Mpixel/s/pin
  - 10mm radius
    - 3.9 Gpixels/s
    - ~50Mpixel/s/pin

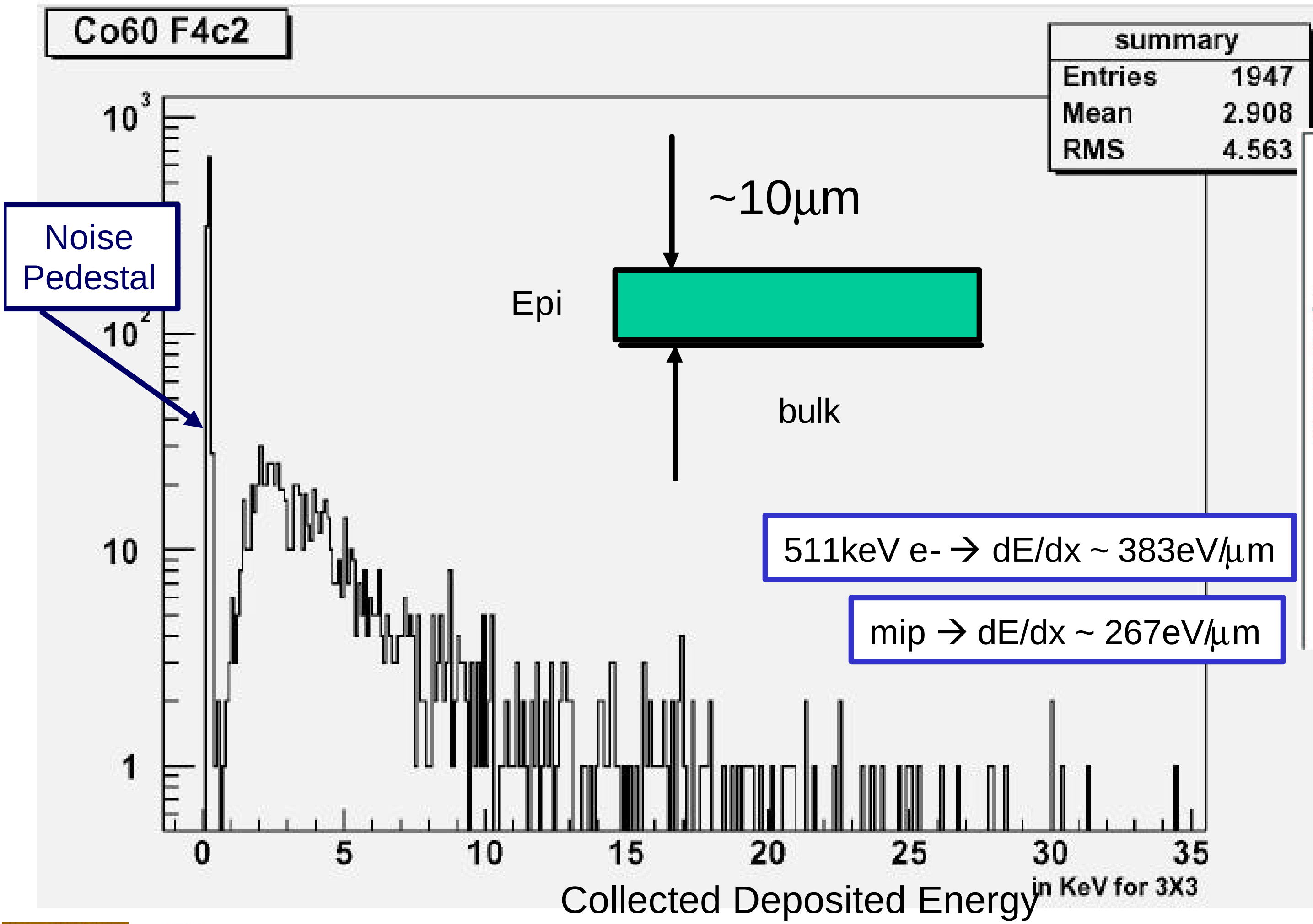
Two ways around:
- Multi-orbit
- "Tiling"

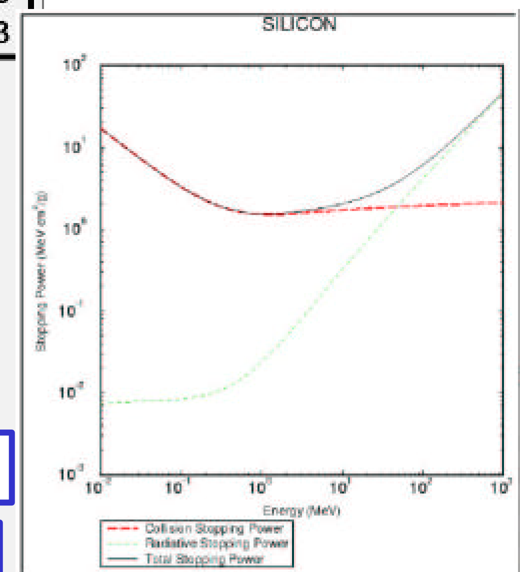
Real max. latency
Set by <L1/L2> rate

What's Next

- Short term goals:
  - Multiple detector operation
    - Hardware in hand, a bit of firmware required
  - CAP2 Evaluation
    - Use CAP1 as a trigger (?)
    - Possibility of very fast sampling
  - Software Development
    - Basics in place
    - Interactive event display (online vs. offline)
  - Beamtest box
    - Fine alignment of multiple CAP1/CAP2 for testing
    - Dark box to avoid heavy metal covers
    - Within a month or two could be ready for beam

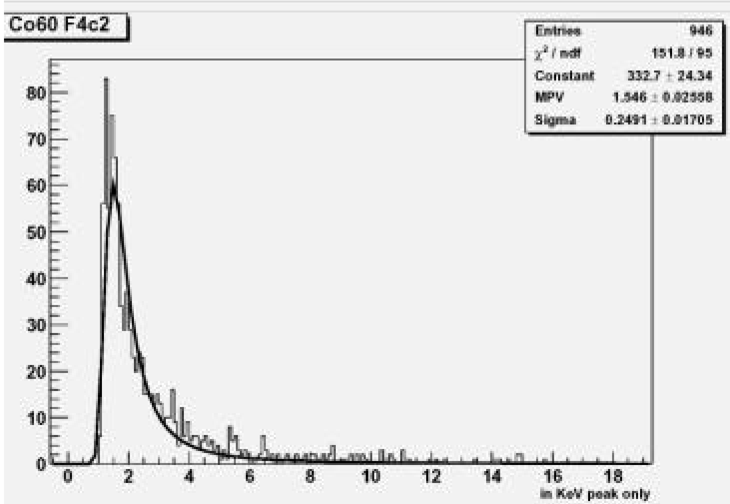
Charge Collection Efficiency (2)

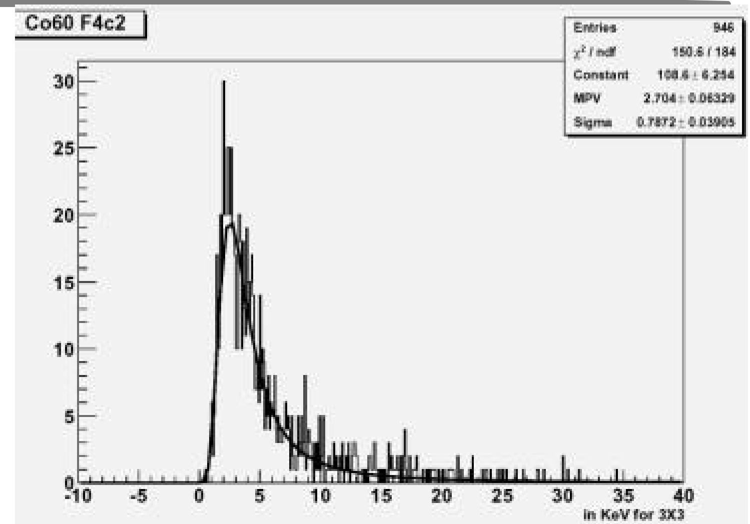


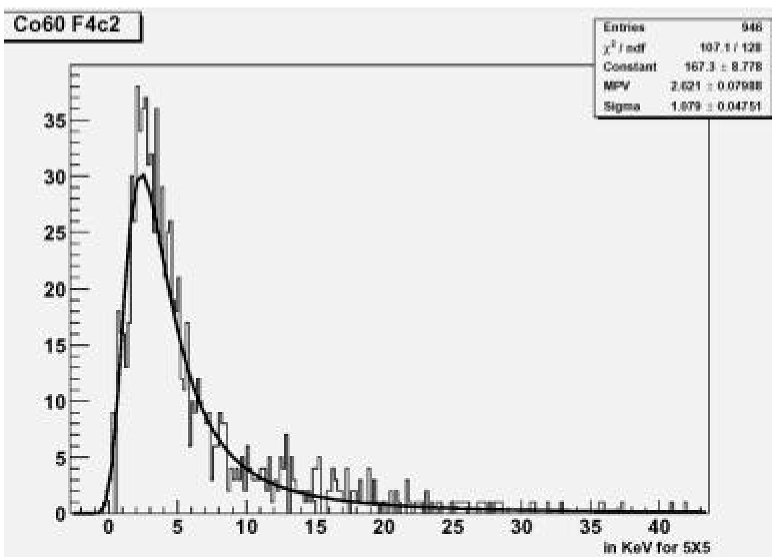


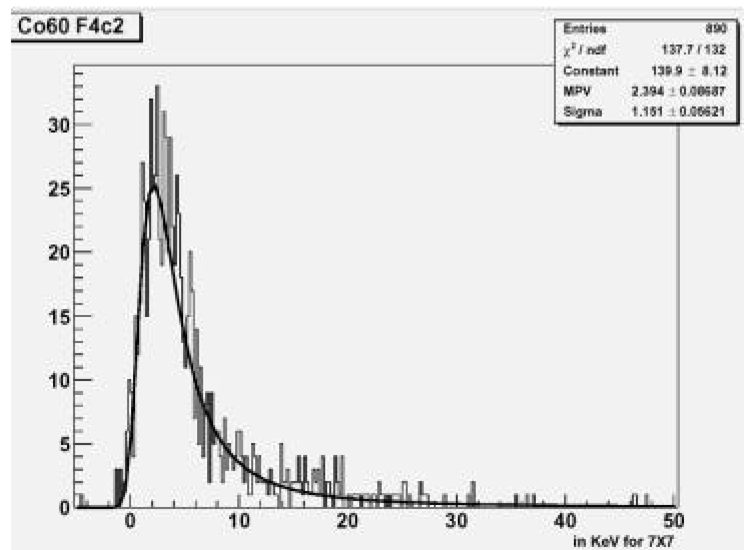
Will Check After Irradiation

Charge Spread









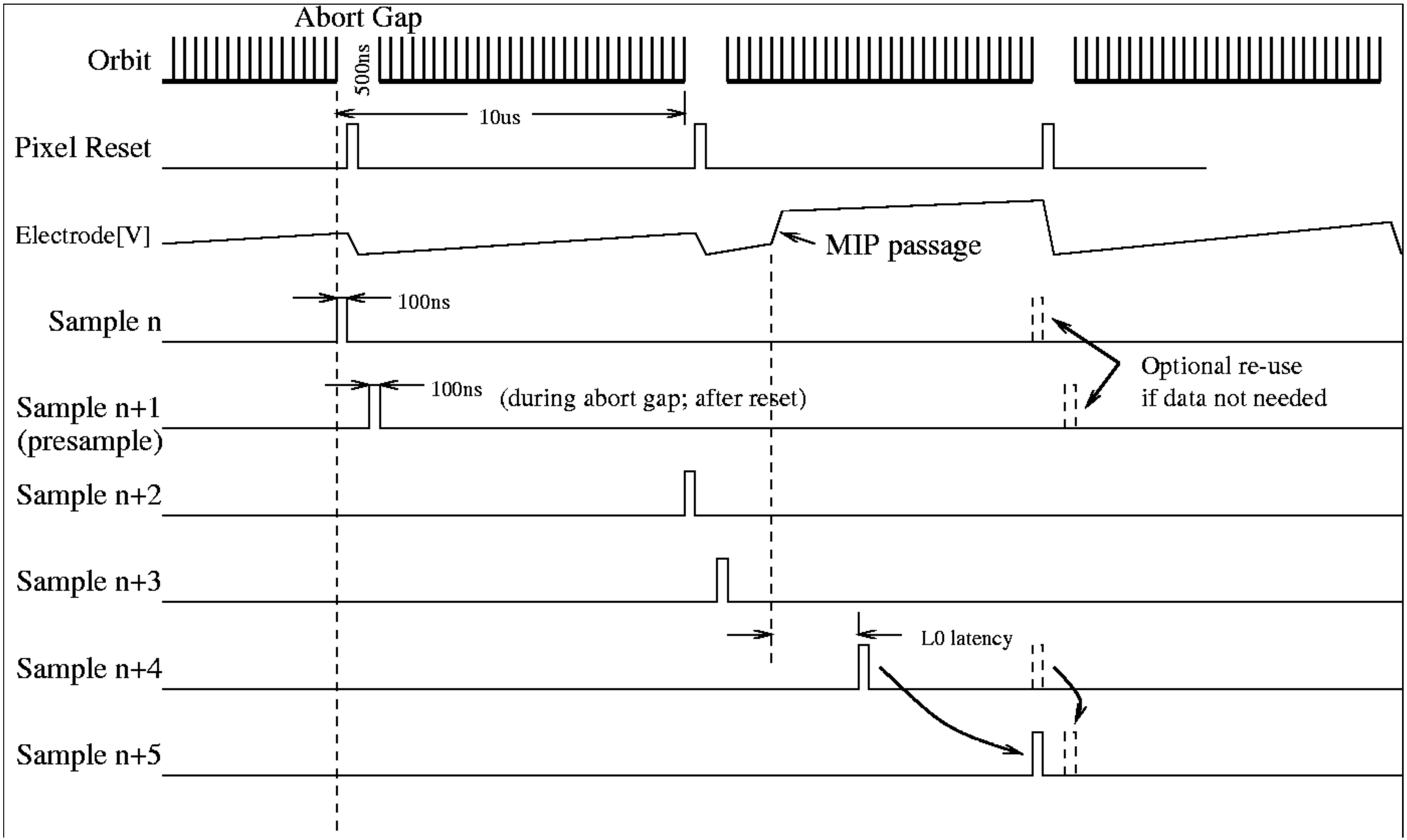
SNR Comparison

SPICE extraction:		3.22	fF	+/- 0.6fF?		Detector:	14	µm			
Q=	1.60E-19	C/e-	Q=C*V			DSSD ref:	300	µm	24000	e-hole pair/m.I.p.	
V=	4.97E-05	V/e-				Geom SF:	0.046667				
chip transfer:		0.78	Vout/Vin			Signal:	1120	e-	max produced		
(SPICE)											
						Collection	0.5	w.a.g. -- in max channel			
Resistive Divider:		1	was 2:1			efficiency					
CAPevF1 amp:		7	gain			Peak signal:	560	e-			
50 ohm series term:		0.5	voltage divide								
CAPevB1 amp:		0.65	gain								
Net transfer gain:		**1.7745**									
Sensitivity:		0.088174	mV/e-			**Expected SNR:**		19.75096			
CAPevB1 noise:		**2.5**	**ADC lsb noise**			**Sigma Set:**	7				
CAPevB1 ADC:		1	mV/lsb			**Threshold:**	60				
CAPevB1 sensitivity:		11.34122	e-/lsb			**m.I.p exp.**	49.37739				
CAPevB1 floor:		28.35306	e-								

Striplet Occupancy Scaling

- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm^2
  - Striplet spatial reduction:
    - Striplet area = 1300μm x 22.5μm ~ 650k μm^2
    - Reduction factor ~6.5
  - Striplet temporal improvement:
    - 1.0μs SVD vs. 100ns Striplet PVD
    - Reduction factor ~ 10
  - Grand total:
    - $10\% * 20 * 6.5^{-1} * 10^{-1}$
    - Can expect ~ 3% occupancy

One Operating Mode



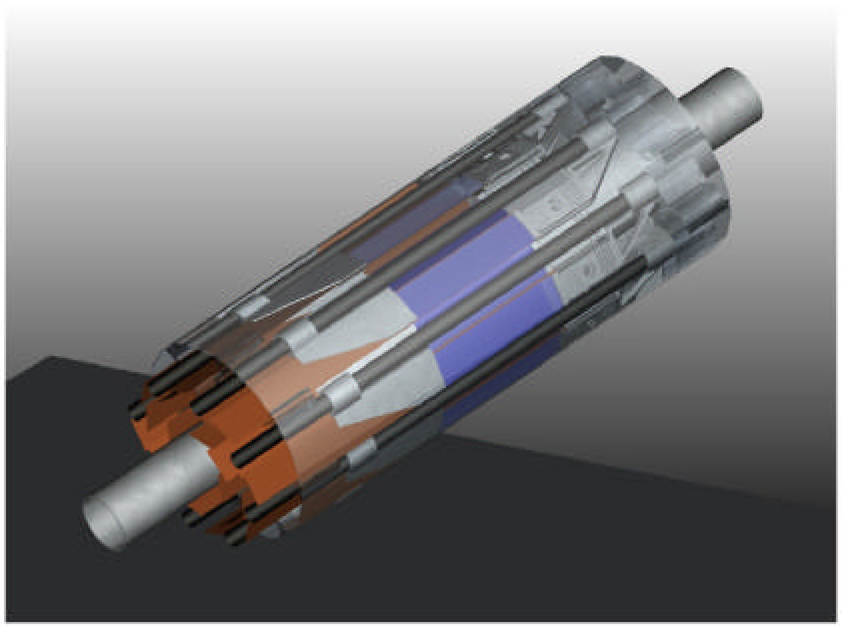
The Bottleneck

- Not trivial, but probably possible to:
  - Sample with adequate SNR
  - Read data off pixel with small enough latency
  - Provide periodic analog resets without incurring deadtime
- However:
  - Not easy to get this torrent to the electronics hut
    - Exploring 2 different fiber optics schemes
    - Custom SiGe mixer/modulator may be a solution
- Looks like can fit everything in one COPPER crate:
  - 1 high-speed fiber/half ladder
  - 1 high-speed fiber/FINESSE
  - Each FINESSE does all CDS/offset calculations
  - CPU does clustering?

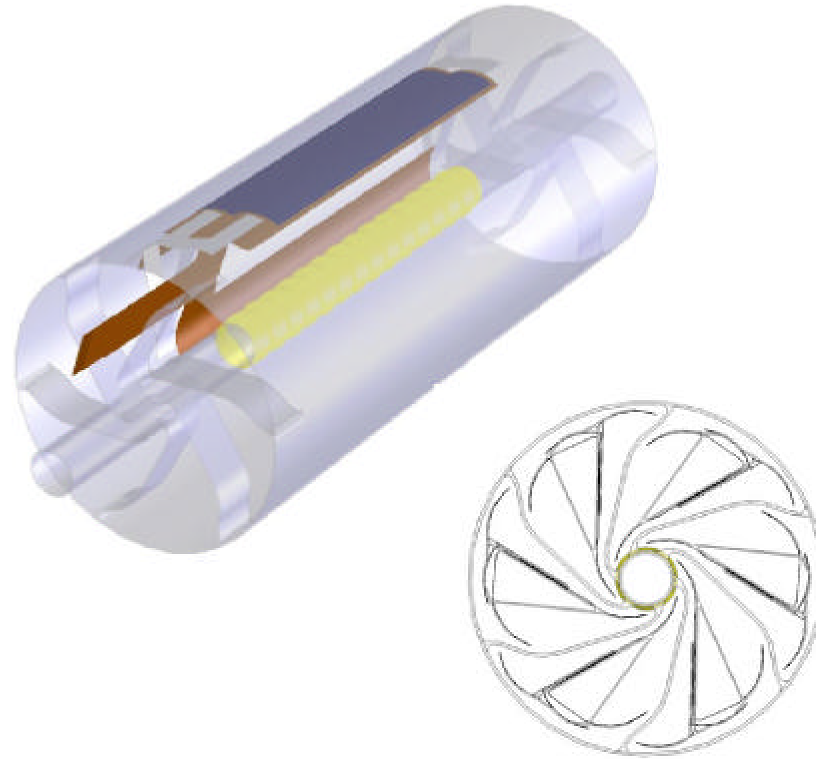
Mechanics

Very preliminary

Mechanical concepts of STAR Micro vertex upgrade using ultra-thin CMOS MAPS *



Tension concept



Self supporting Venetian blade concept

* Curtsey to Howard Wieman, LBL, STAR group