Development of a Monolithic Active Pixel Detector for a Super B Factory - the CAP series

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On behalf of the Belle Pixel Group

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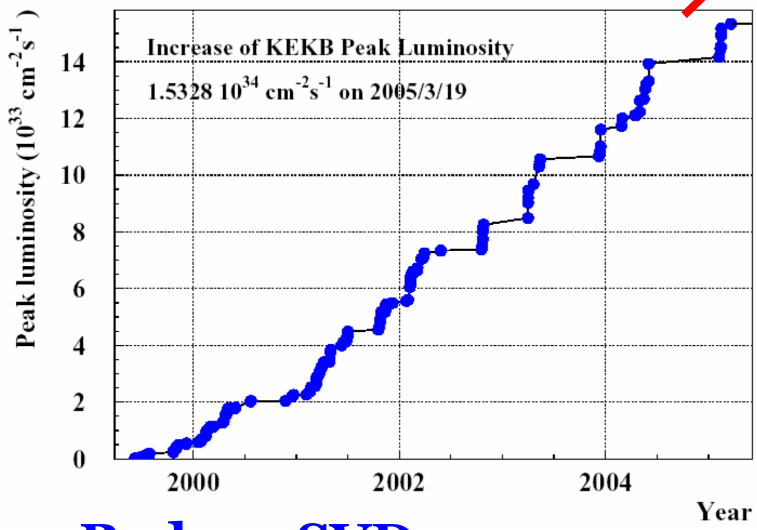
HEP2005 Lisbon

Motivation for Pixels at Super B

SuperKEKB luminosity increase:
L~1.6 x 10^{34} → L~5 x 10^{35} cm^{-2}.s^{-1}



1. Reduce SVD occupancy

Present : layer 1 of SVD

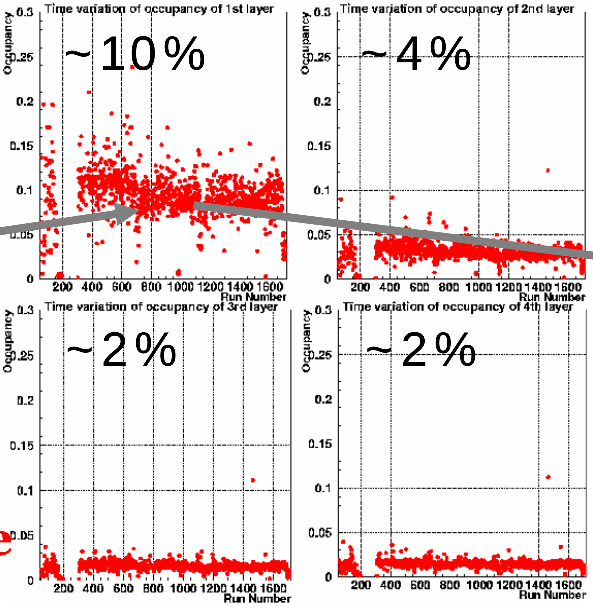
~10% occupancy / 200 Krad.yr^{-1}

Upgrade: Super-Belle

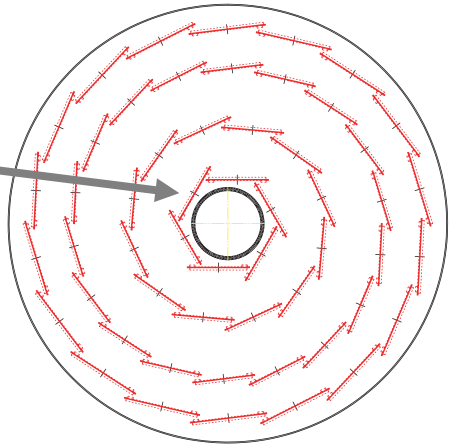
~ 20 – 50 x (?) expected increase

Conventional solutions (Si strips) will not work…

Other alternatives include "striplets" and APV25 chip



Present:
Belle SVD2



Natural alternative - Pixel type sensor

Requirements

1. Low occupancy
2. Fast Readout Speed
3. Radiation Hardness
4. Thin Sensor
5. Full-sized detector prototype

R&D steps

Technology Choice — XTEST2, LHC hybrid pixels

↓ MAPS

Prototypes

CAP1 – basic functionality — Jun. 2004 @ KEK

↓

CAP2 – pipelined readout — T943 Dec. 2004 @ FNAL

↓

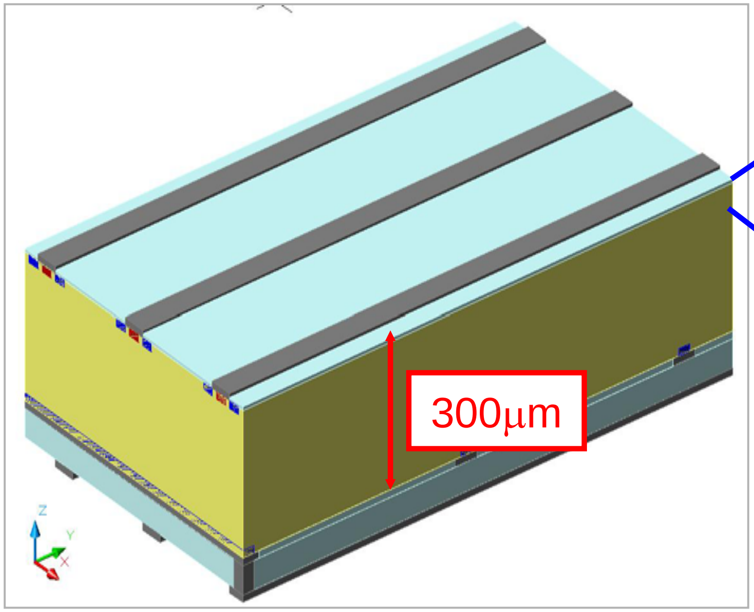
CAP3 – full-size/speed — Autumn 2005 (expected)

↓ Preliminary Design Report

PVD1.0
- ➔ Near Term (SVD2 Layer 1 drop-in)
- ➔ IR upgrade

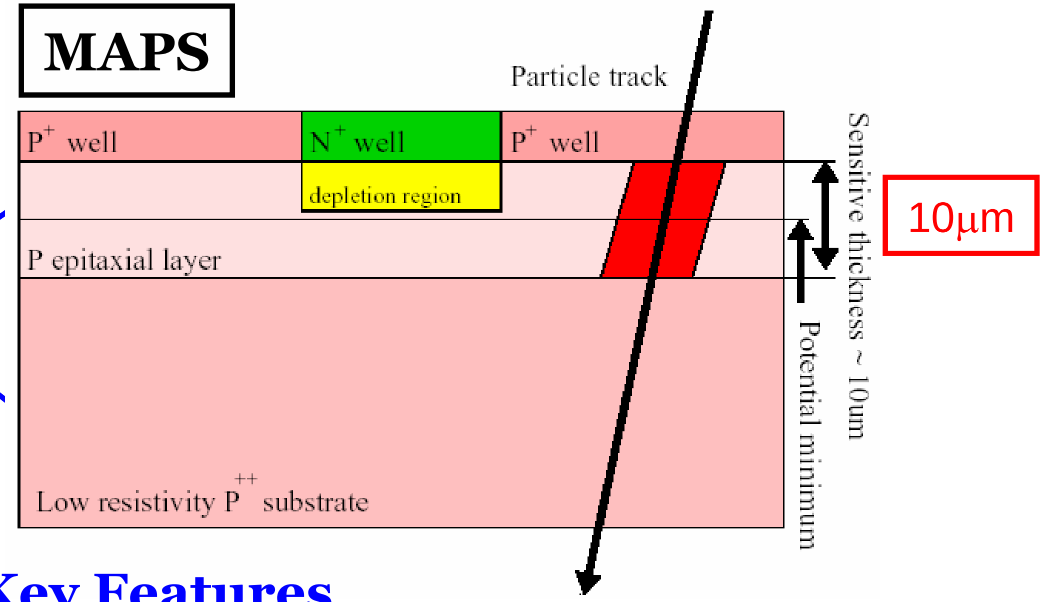
Candidate: Monolithic Active Pixel Sensor

Current DSSD



Because of large capacitance, DSSDs thick -- MAPS can be made VERY thin

MAPS

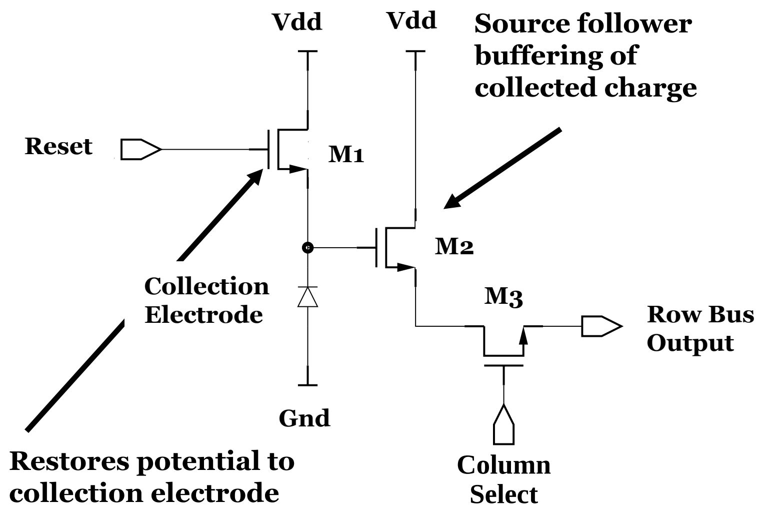


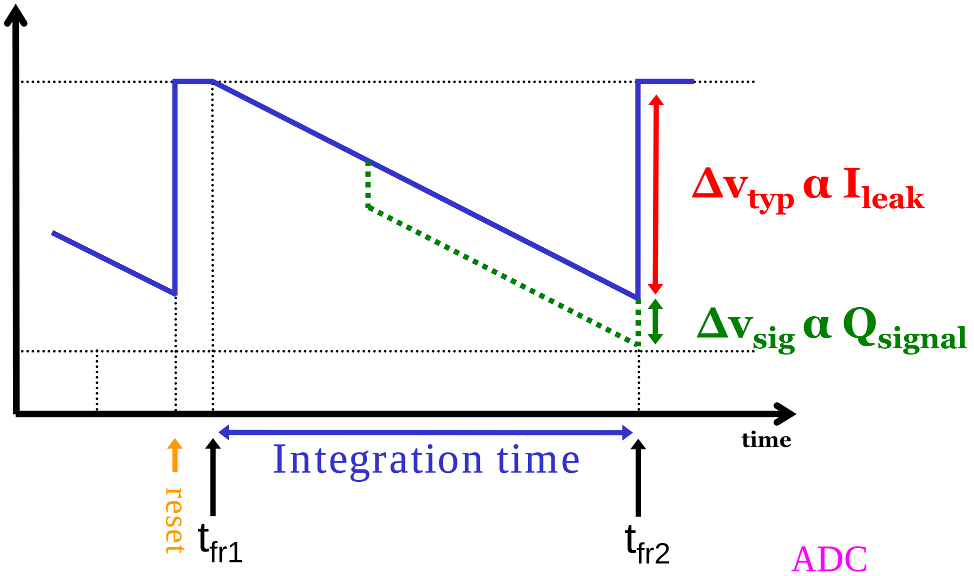
Key Features

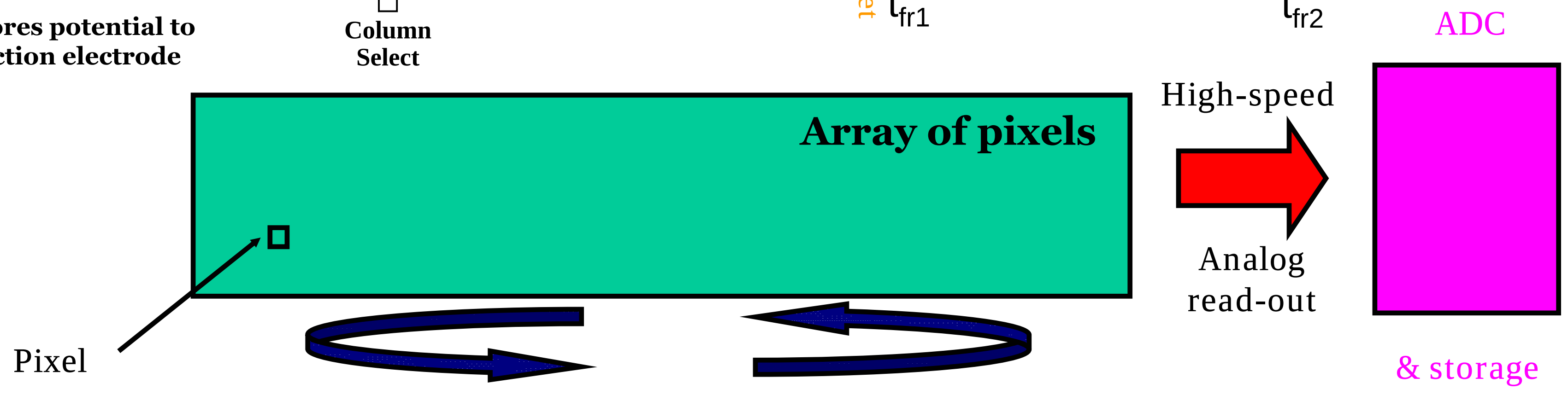
- Thermal charge collection (no HV)
- Thin - reduced multiple-scattering, γ conversion, background γ target
- NO bump bonding – fine pitch possible (8000 x geometrical reduction)
- Standard CMOS process - “System on a Chip” possible (TSMC 0.35 and 0.25µm)

Continuous Acquisition Pixel (CAP) Concept

Based on 3 transistor cell

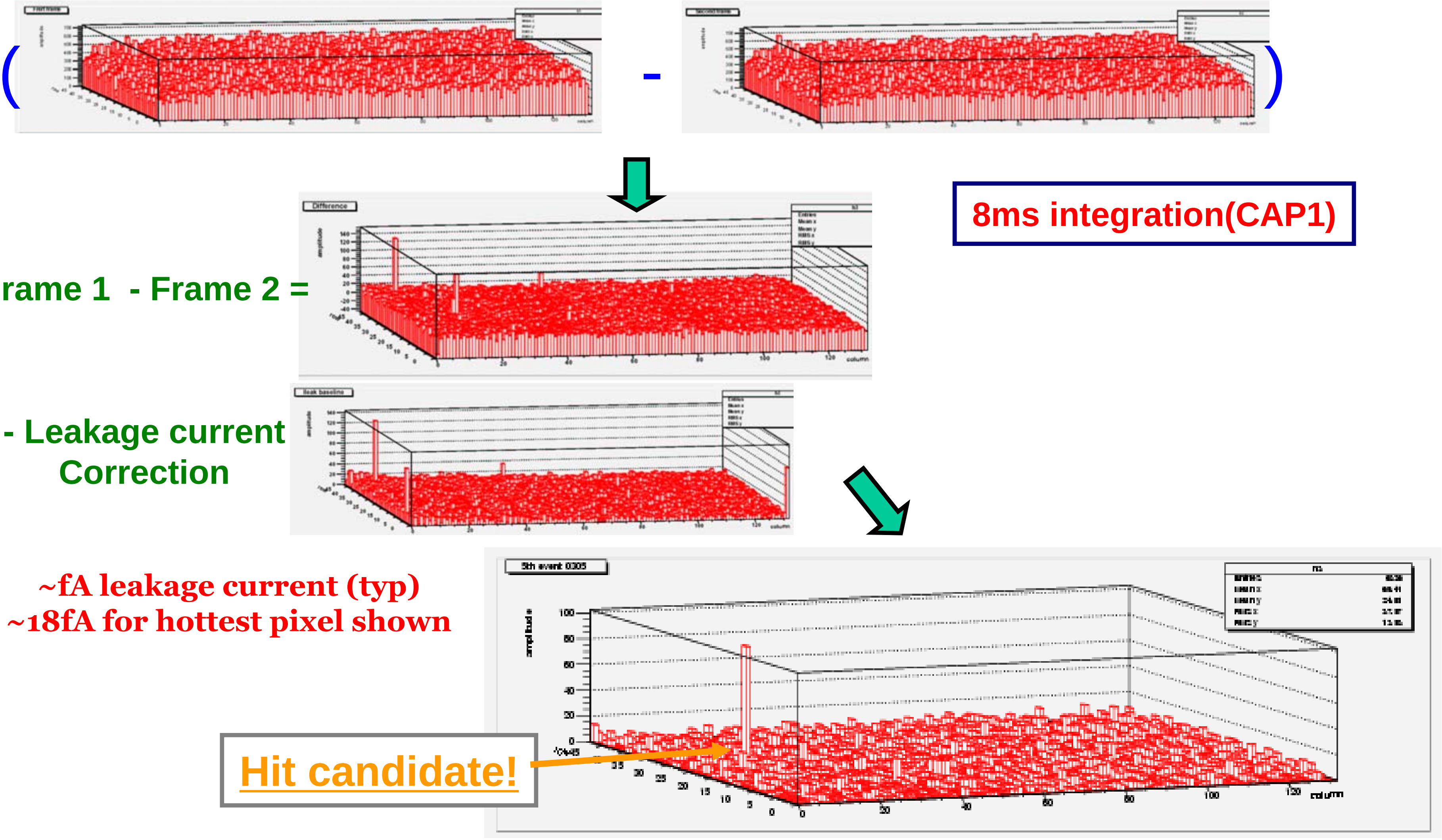






Pixel Array: Column select – ganged row read

Correlated Double Sampling (CDS)



8ms integration(CAP1)

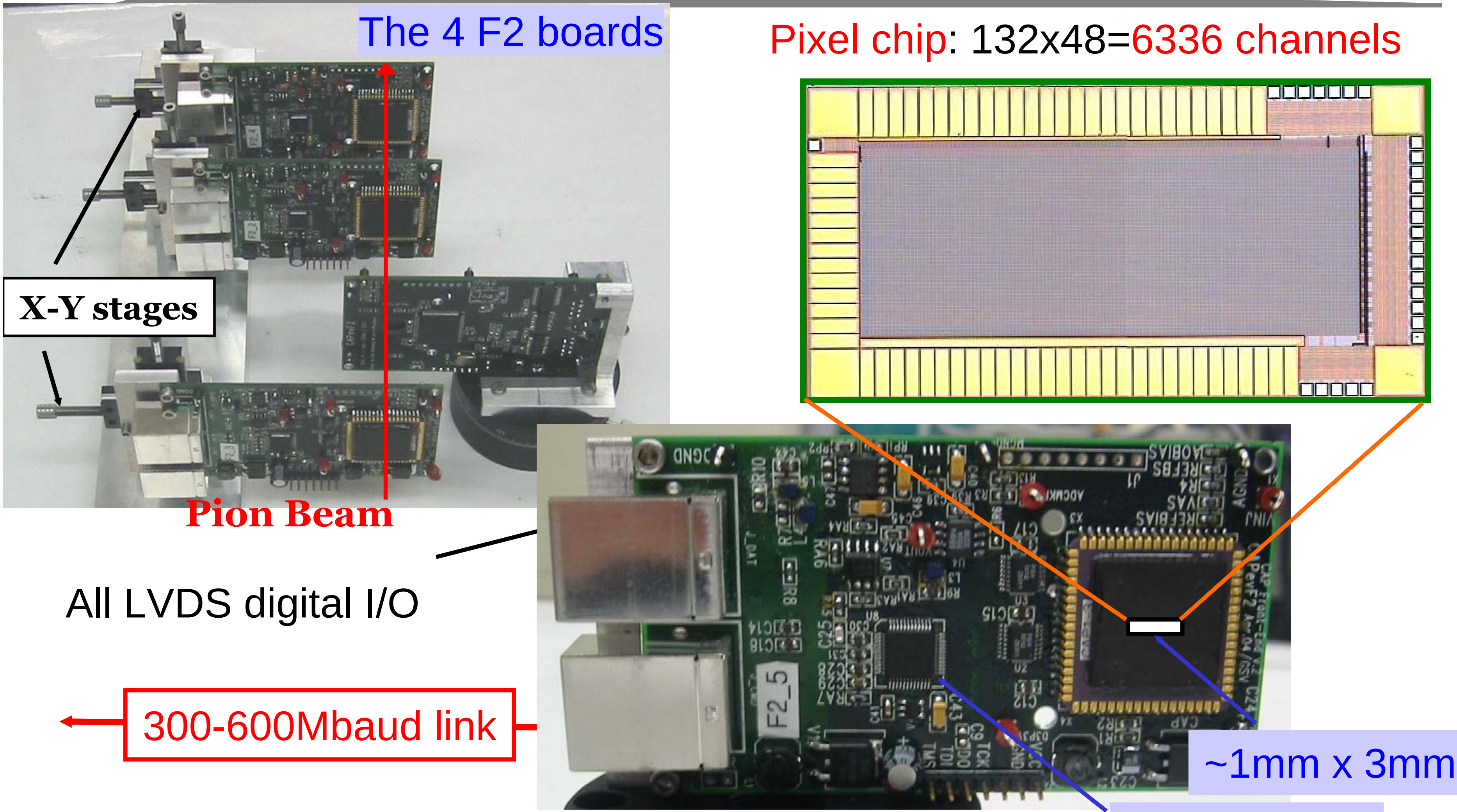
Frame 1 - Frame 2 =

- Leakage current Correction

~fA leakage current (typ)
~18fA for hottest pixel shown

Hit candidate!

CAP1: basic operation confirmed in a test beam experiment at KEK



The 4 F2 boards

X-Y stages

Pion Beam

Pixel chip: 132x48=6336 channels

All LVDS digital I/O

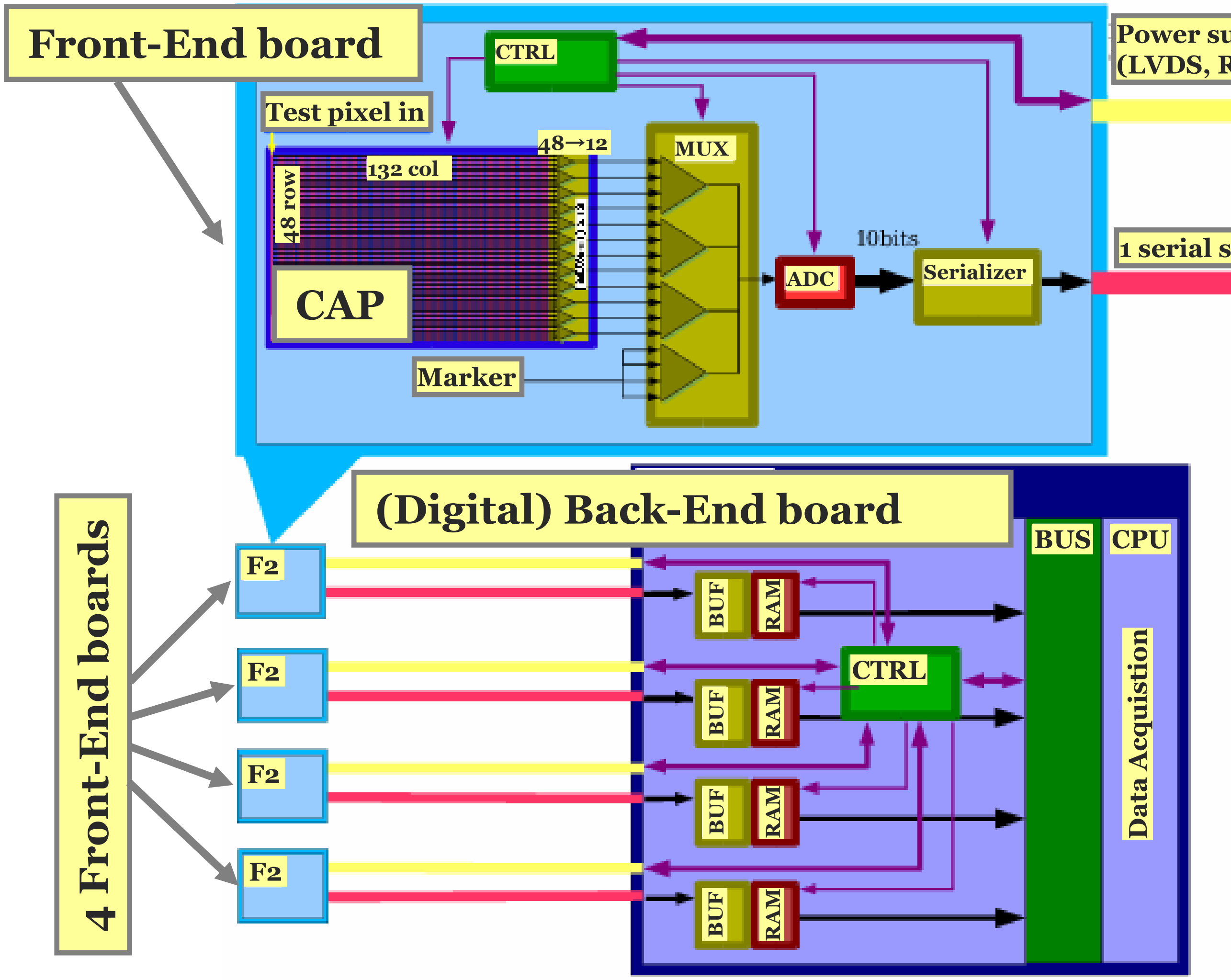
300-600Mbaud link

~1mm x 3mm

On board ADC

Self triggering prototype

CAP1/2 system overview



Front-End board

Power supply & control lines (LVDS, RJ45)

Test pixel in

CTRL

48→12

132 col

48 row

MUX

CAP

10bits

ADC

Serializer

1 serial signal (LVDS, RJ45)

Marker

4 Front-End boards

F2

F2

F2

F2

(Digital) Back-End board

BUS

CPU

BUF

RAM

CTRL

Data Acquistion

Highlights:

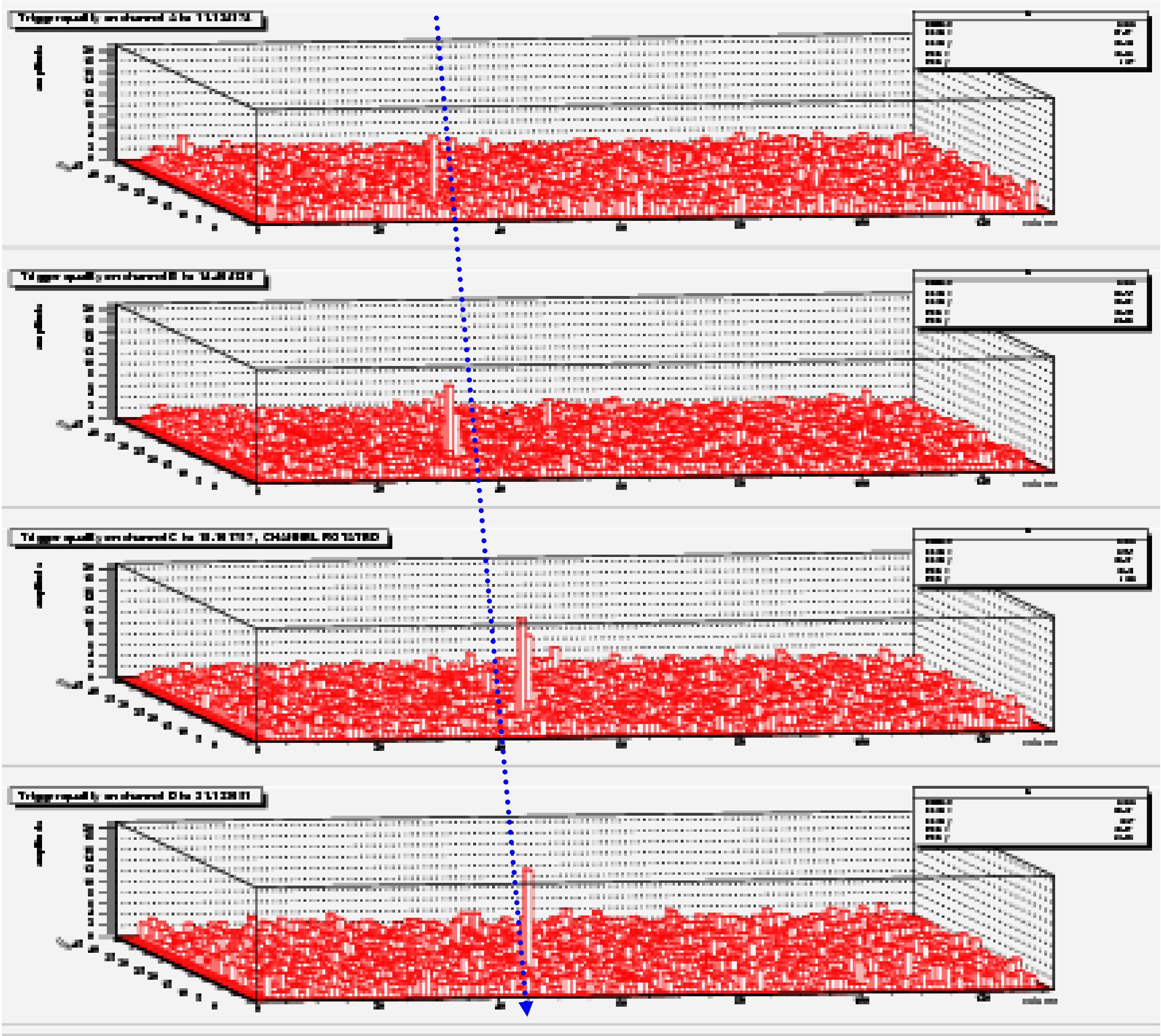
Front-End board:

MUX, ADC, serializer, CPLD

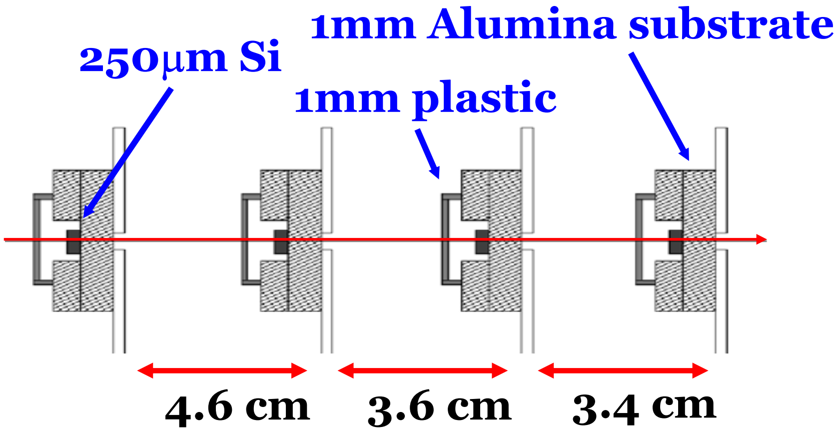
Back-End board: cPCI

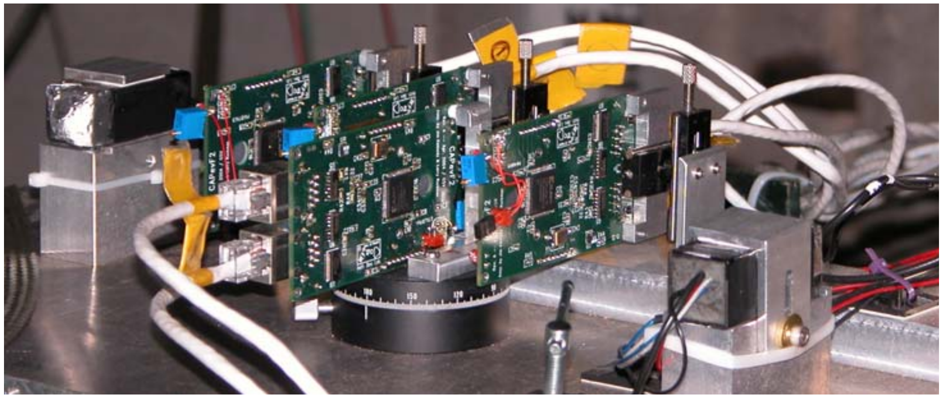
RAM, 5 CPLDs, CPU

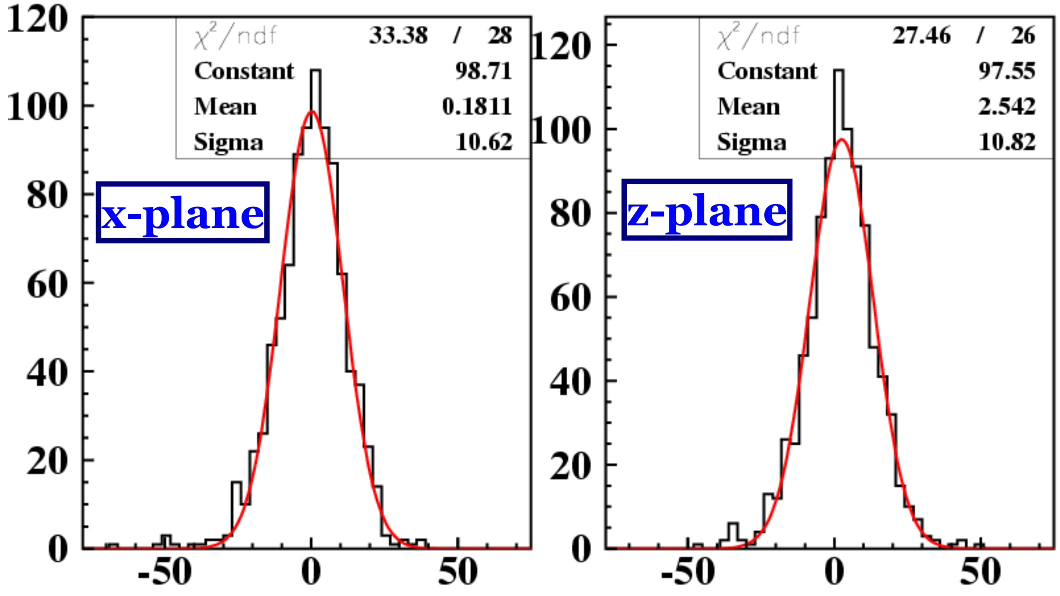
KEK Beam Test: Correlated hits in all 4 layers

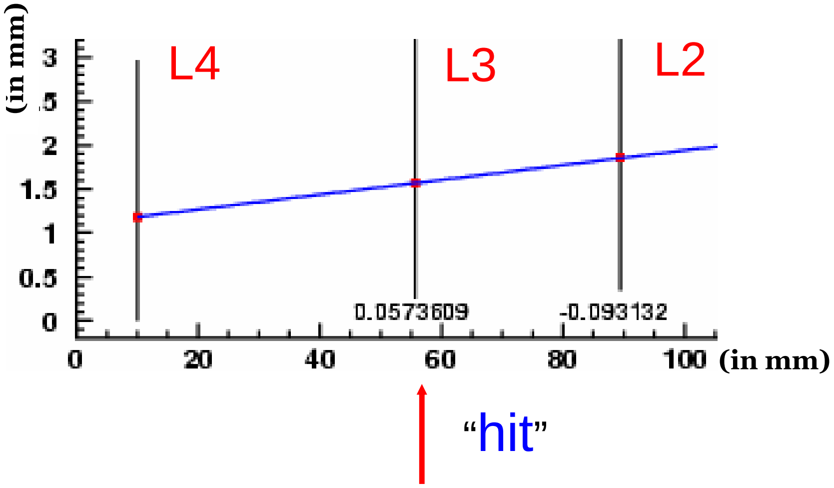


Hit resolution measurement/UL



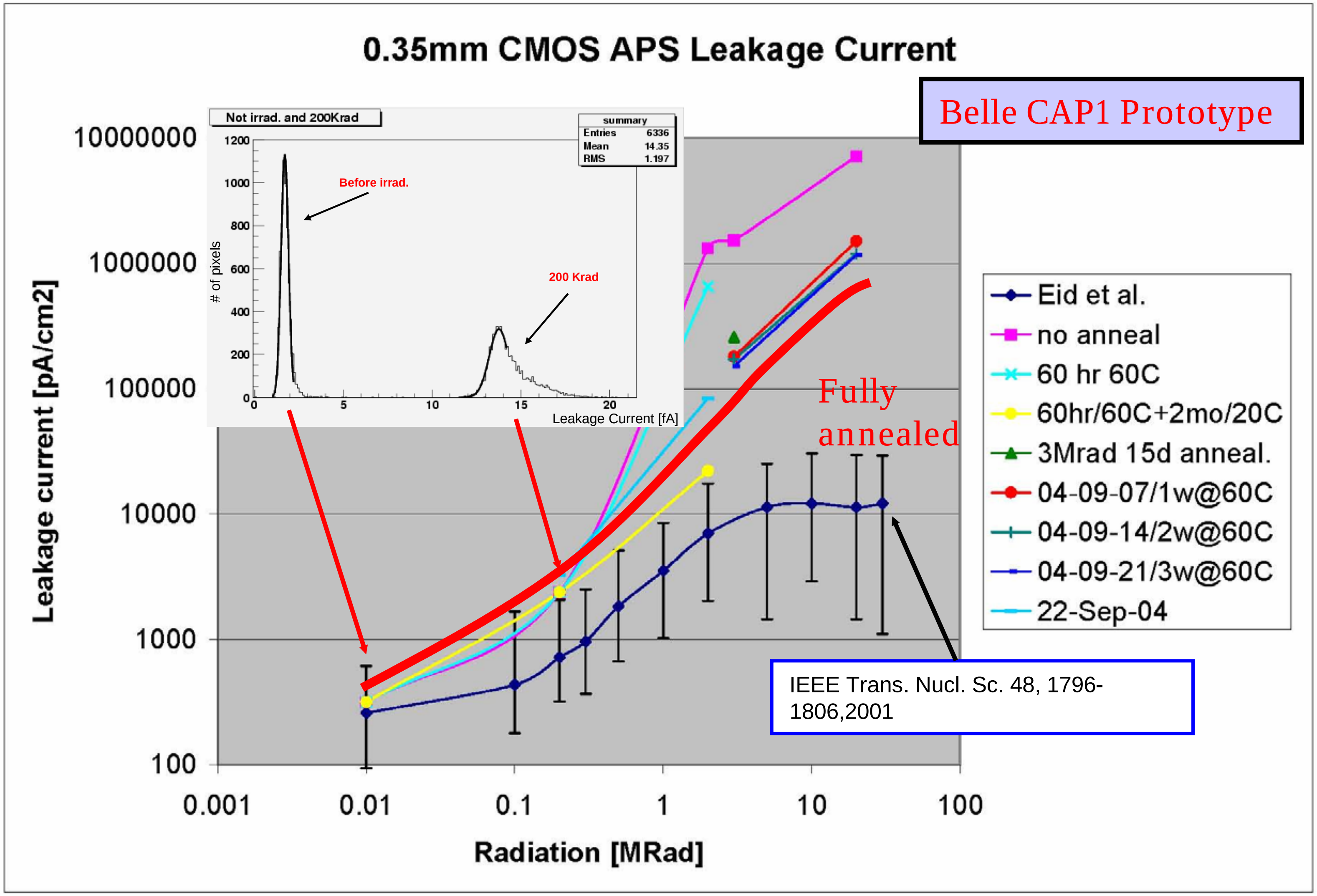






Residuals for 4GeV/c pions:
< 11µm (in both planes)

Radiation damage results

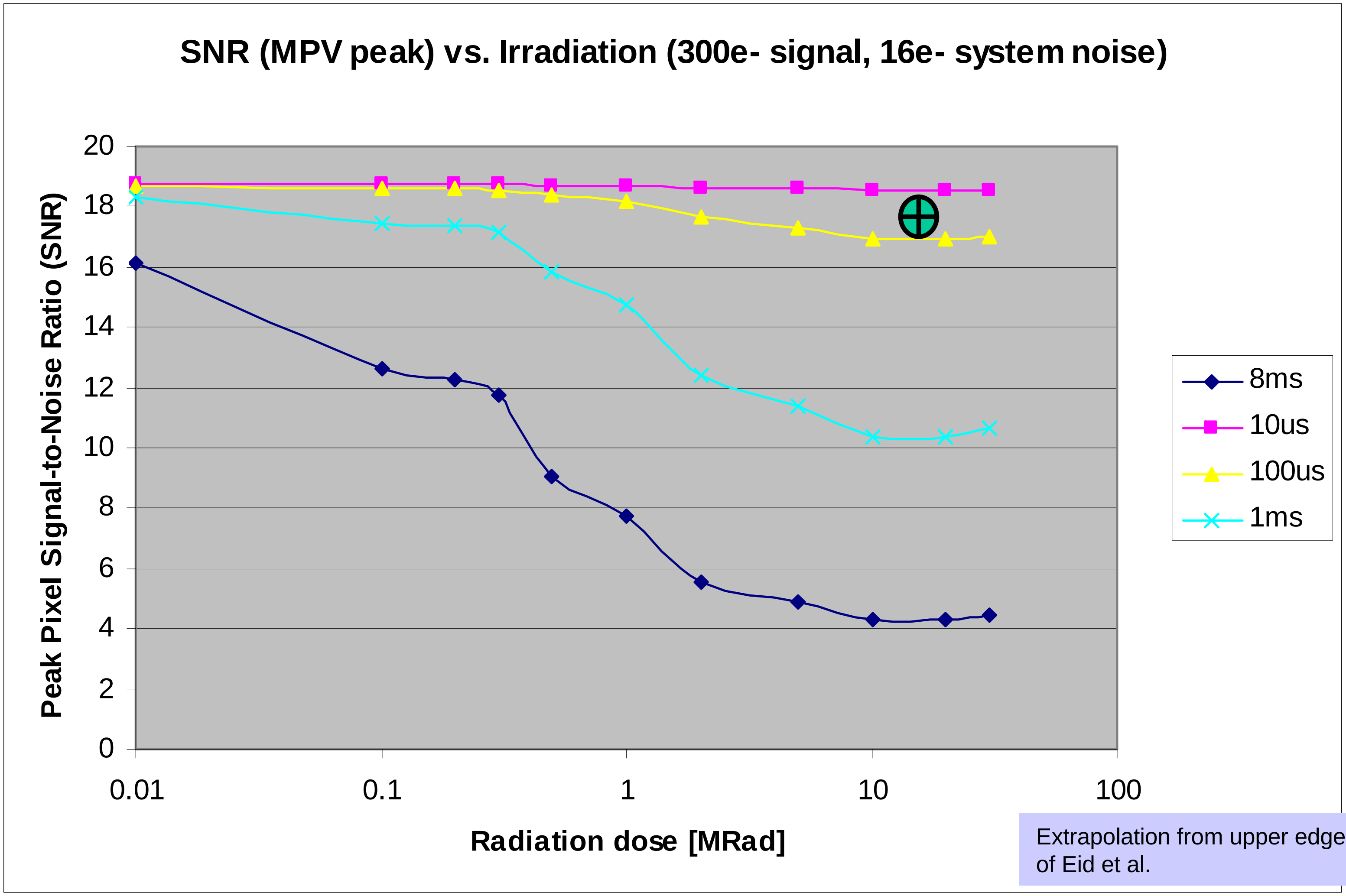


Belle CAP1 Prototype

Fully annealed

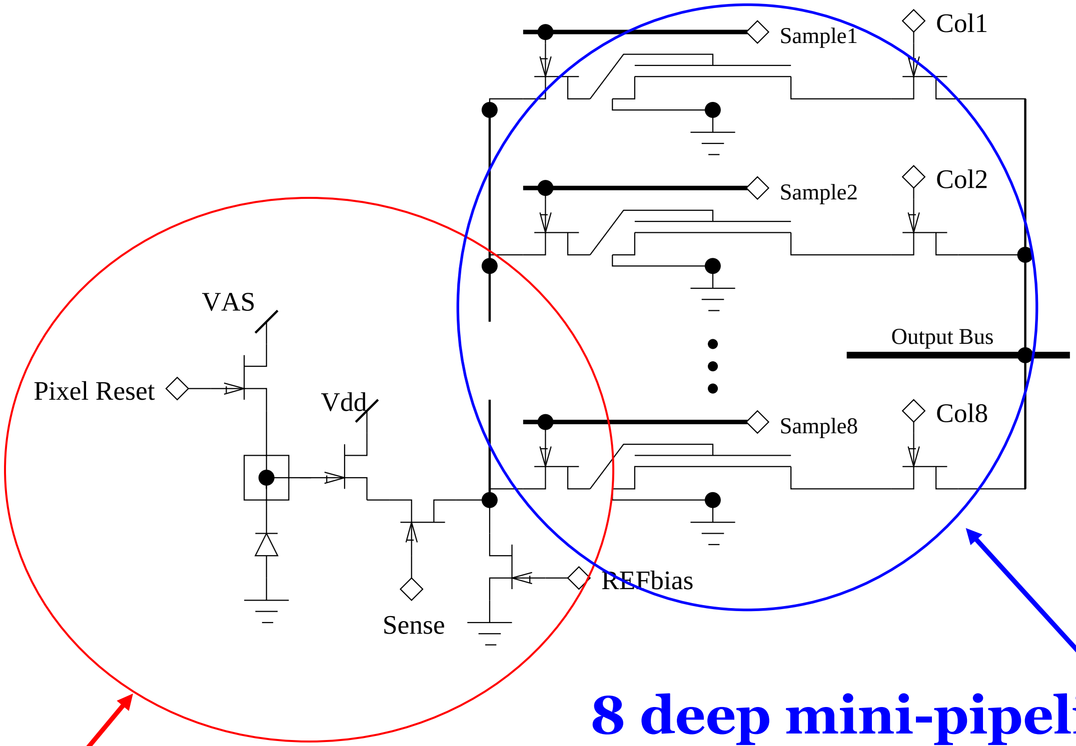
IEEE Trans. Nucl. Sc. 48, 1796-1806,2001

Prediction of Peak pixel S/N vs Dose



Extrapolation from upper edges of Eid et al.

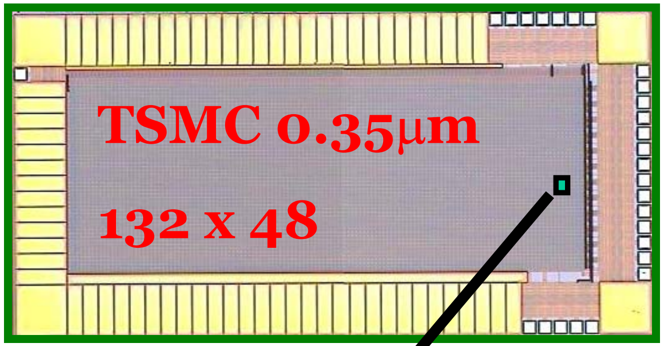
CAP2 – Pipelined operation

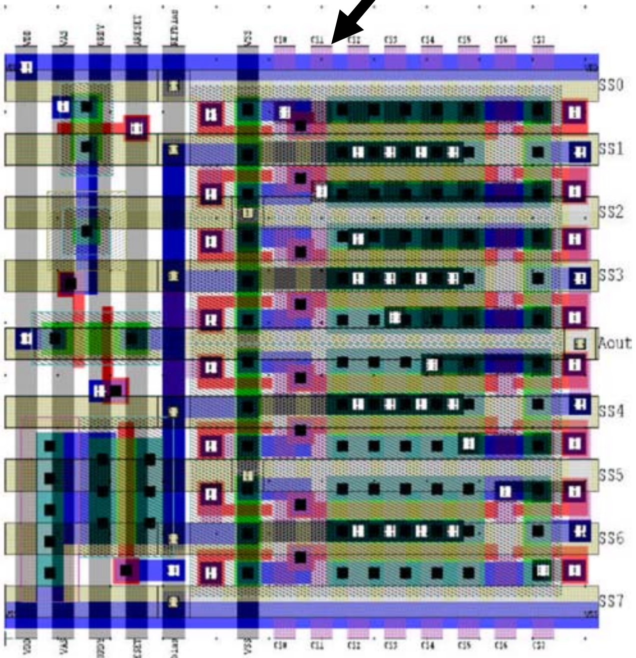


8 deep mini-pipeline in each cell

3-transistor cell

132x48=6336 channels 50688 samples





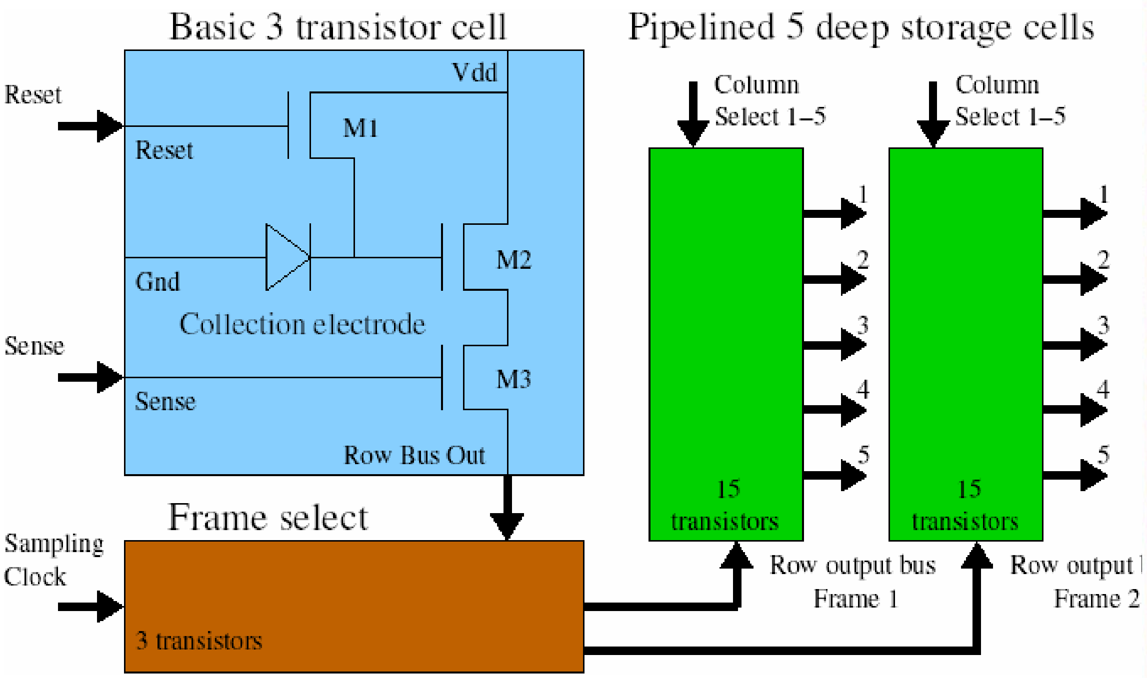
Pixel size 22.5 µm x 22.5 µm

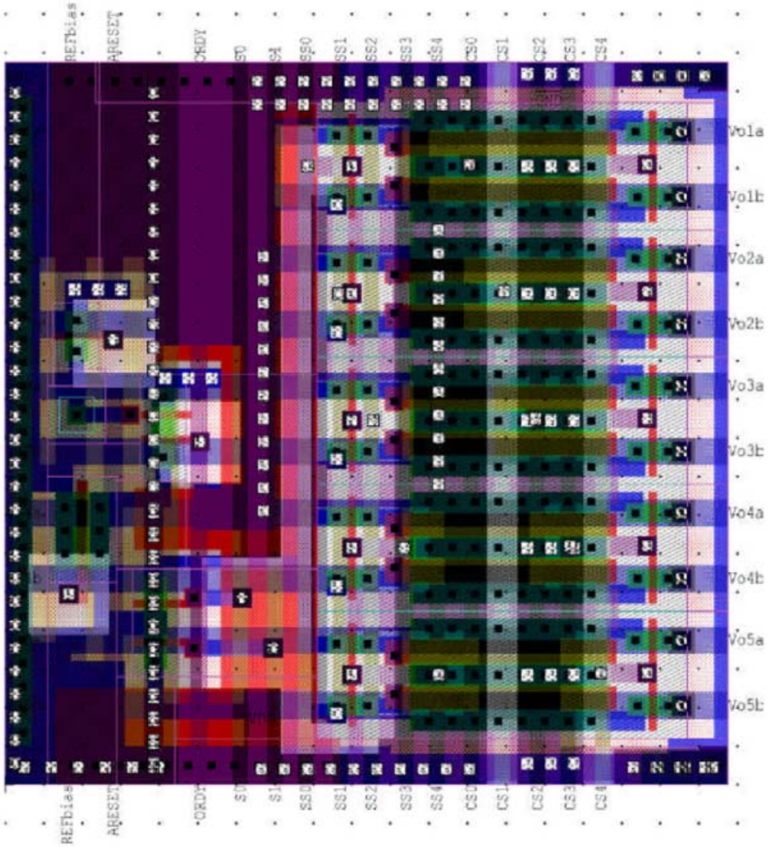
10µs frame acquisition speed achieved!

CAP3 – *Full scale* *pipelined prototype*

5-deep ***double*** pipeline

TSMC 0.25μm Process





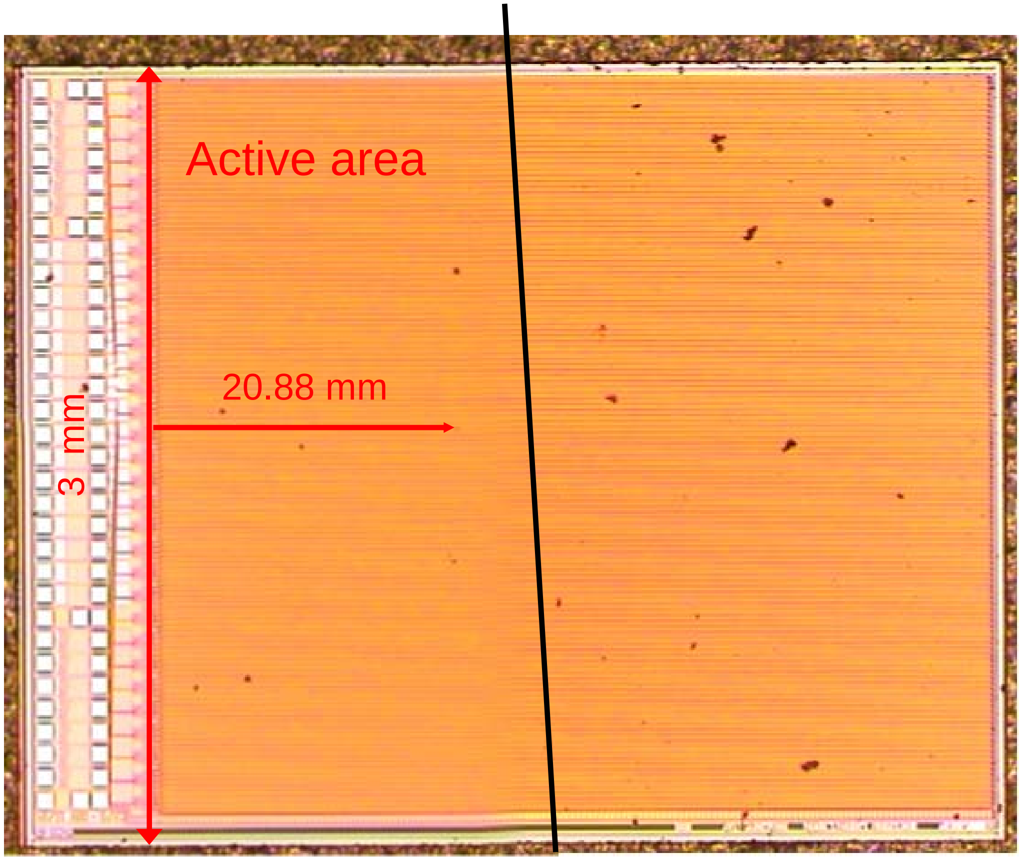
36 transistors/pixel

5 sets CDS pairs

5 metal layers

CAP3 - sensor layout and scale

21 mm

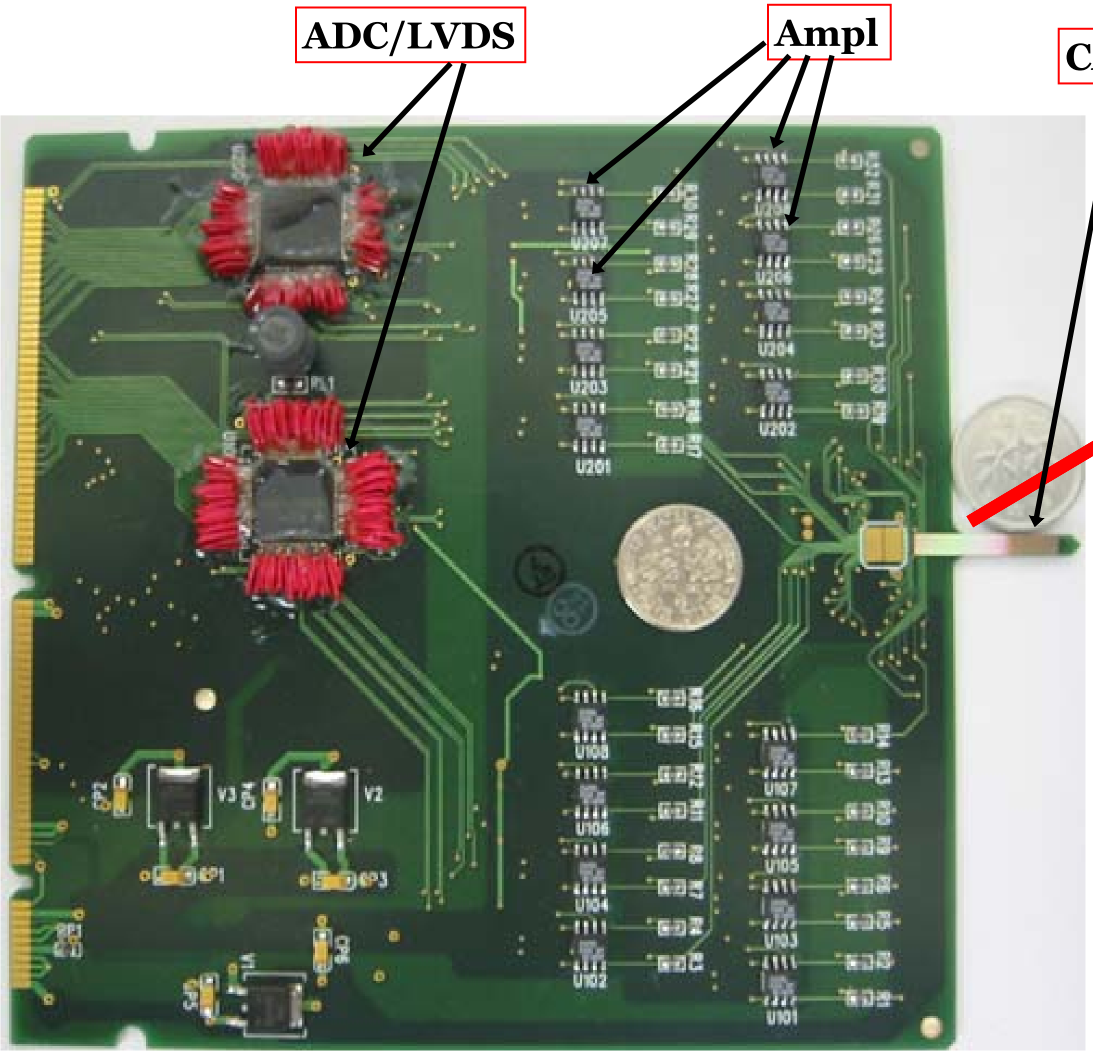


>93% active without active edge processing

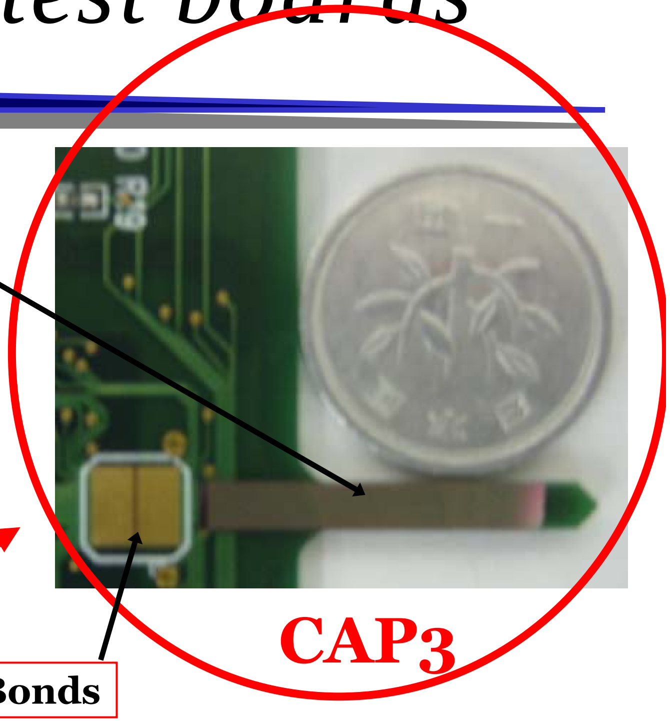
928 x 128 pixels = 118,784

~4.3M transistors !

CAP3 front-end readout test boards

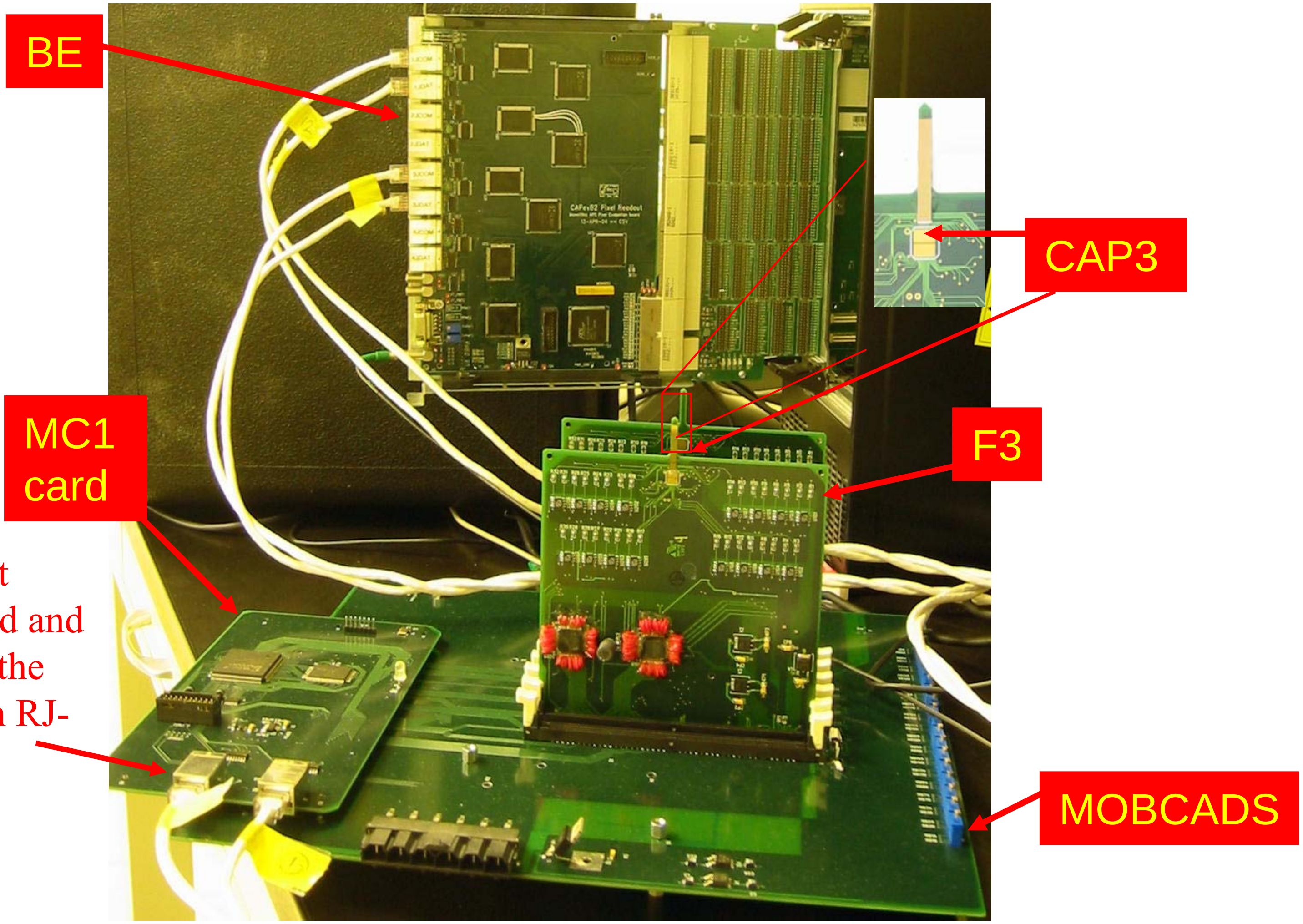


F3 board



- Laboratory testing of the F3 frontend readout board is under way
- Working on the firmware

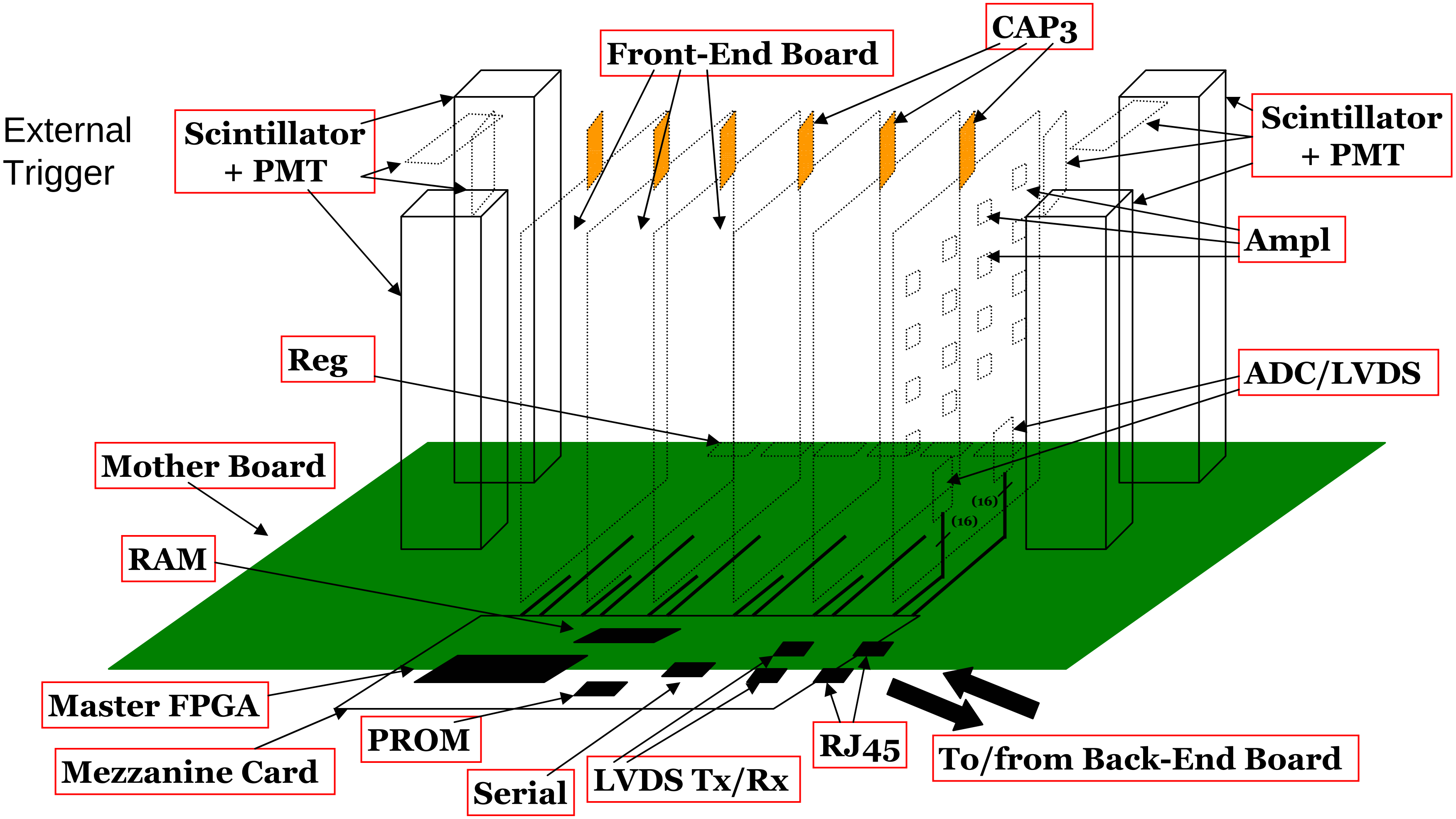
Test setup for CAP3 sensors



Multiplex and sends to BE

Serialized data out from the MC1 card and control signals to the MC1 card through RJ-45 connectors.

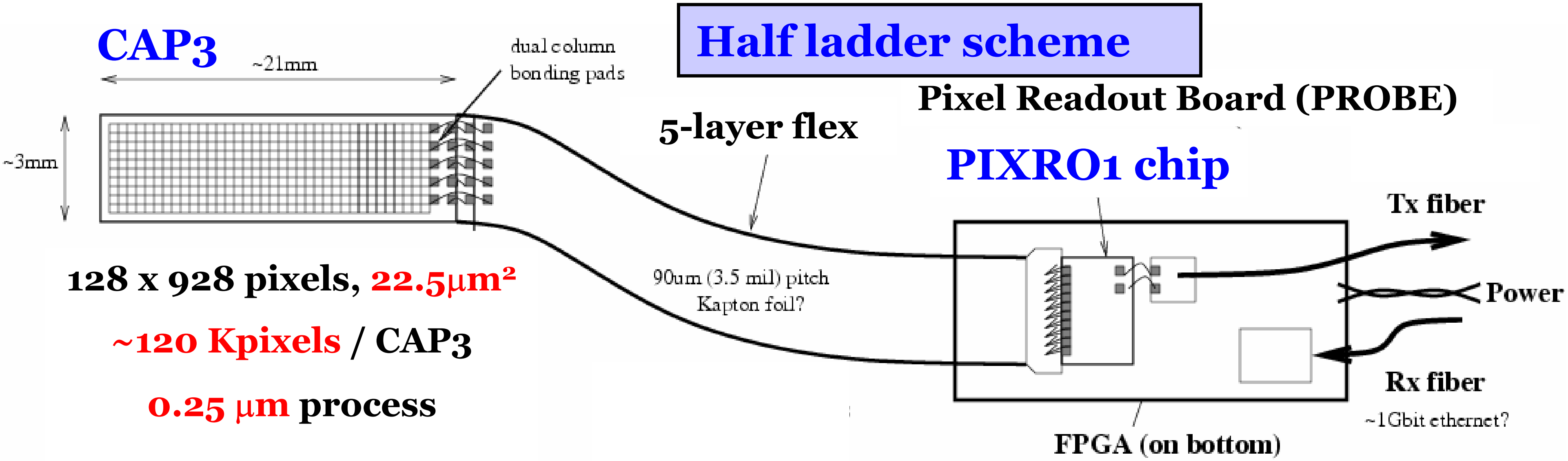
CAP3 test system overview



All these components sit on a movable table

CAP3 based full detector concept

Half ladder scheme

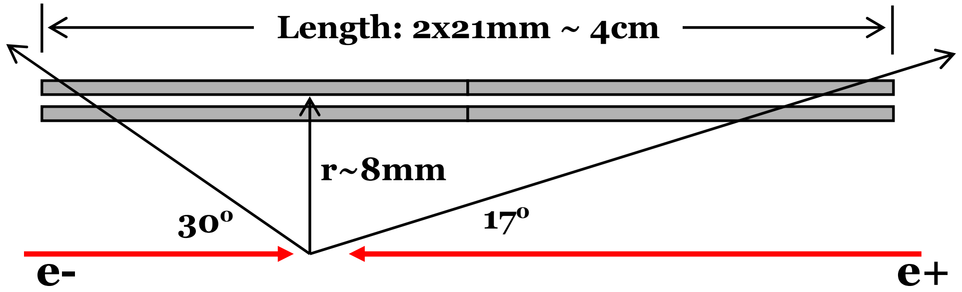


128 x 928 pixels, 22.5μm²

~120 Kpixels / CAP3

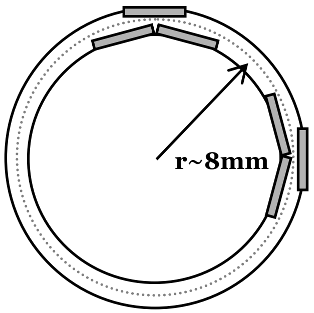
0.25 μm process

Side view



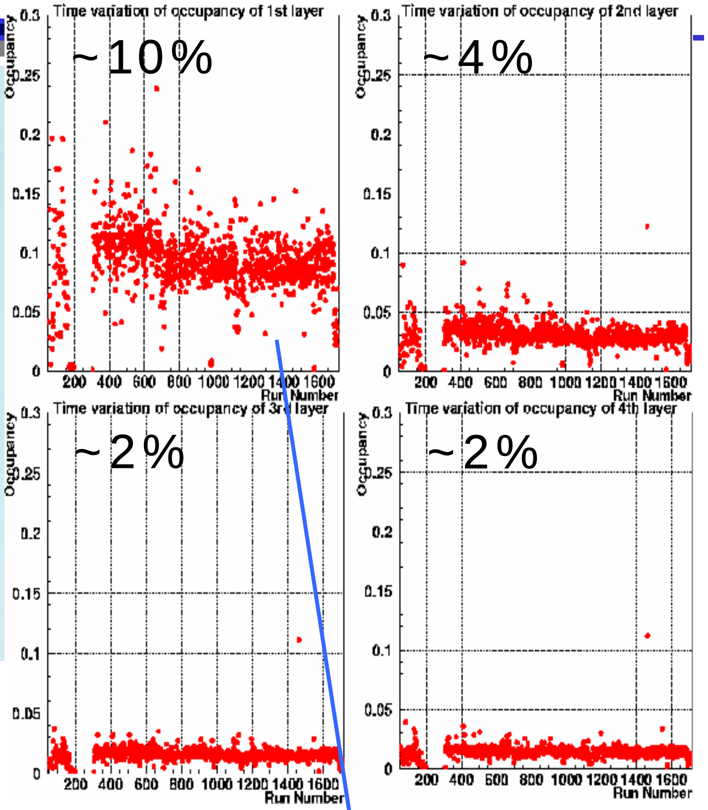
End view

Double layer, offset structure

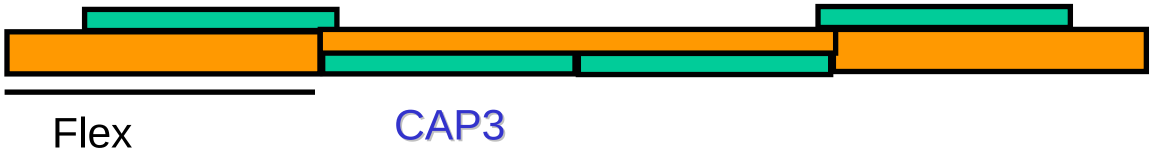


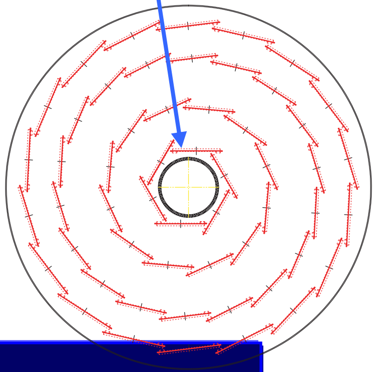
# of Detector / layer ~ 32

Short-term Upgrade

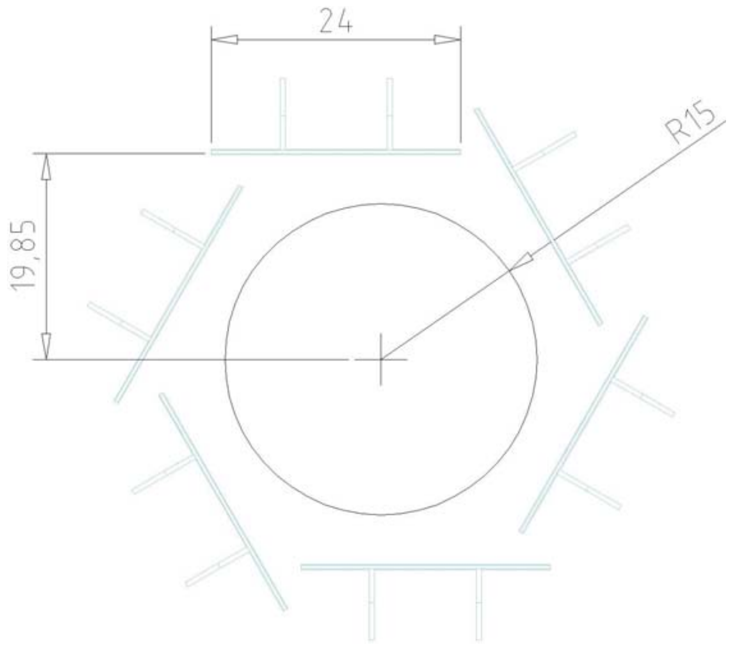


Replace Layer 1 with CAP3 pixels
Mechanically identical (drop in)

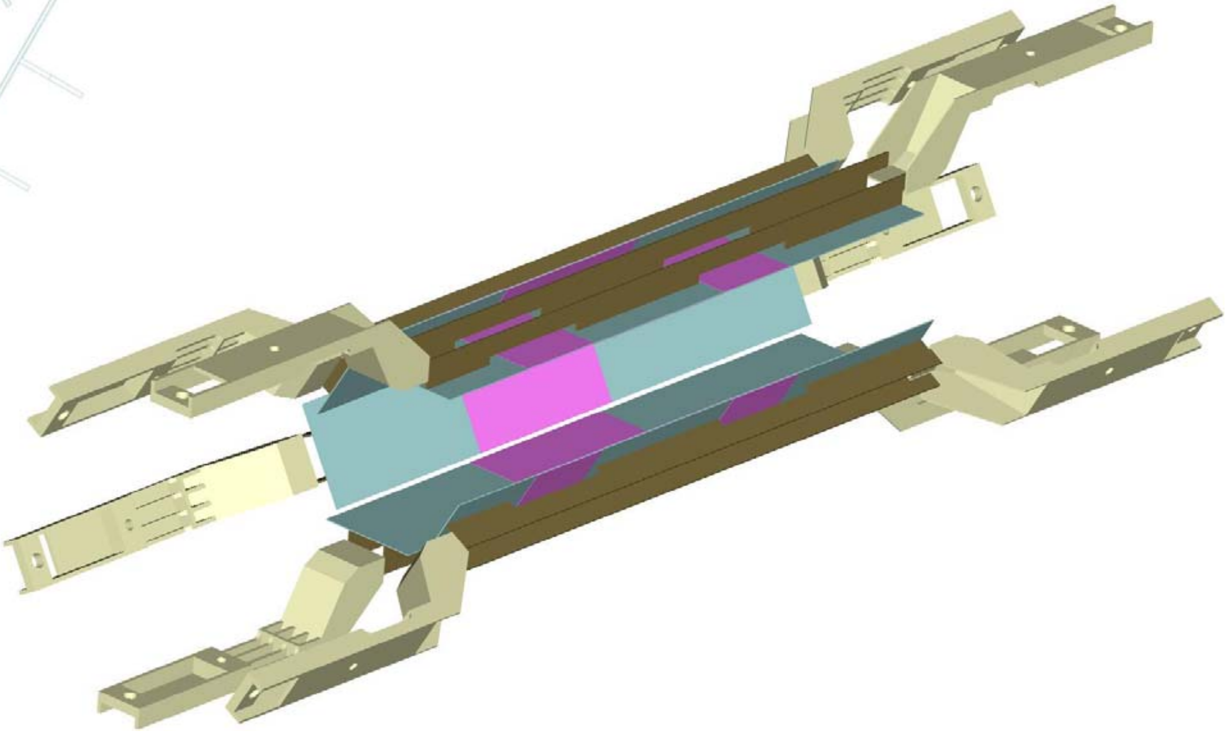




Short-term Upgrade (2)

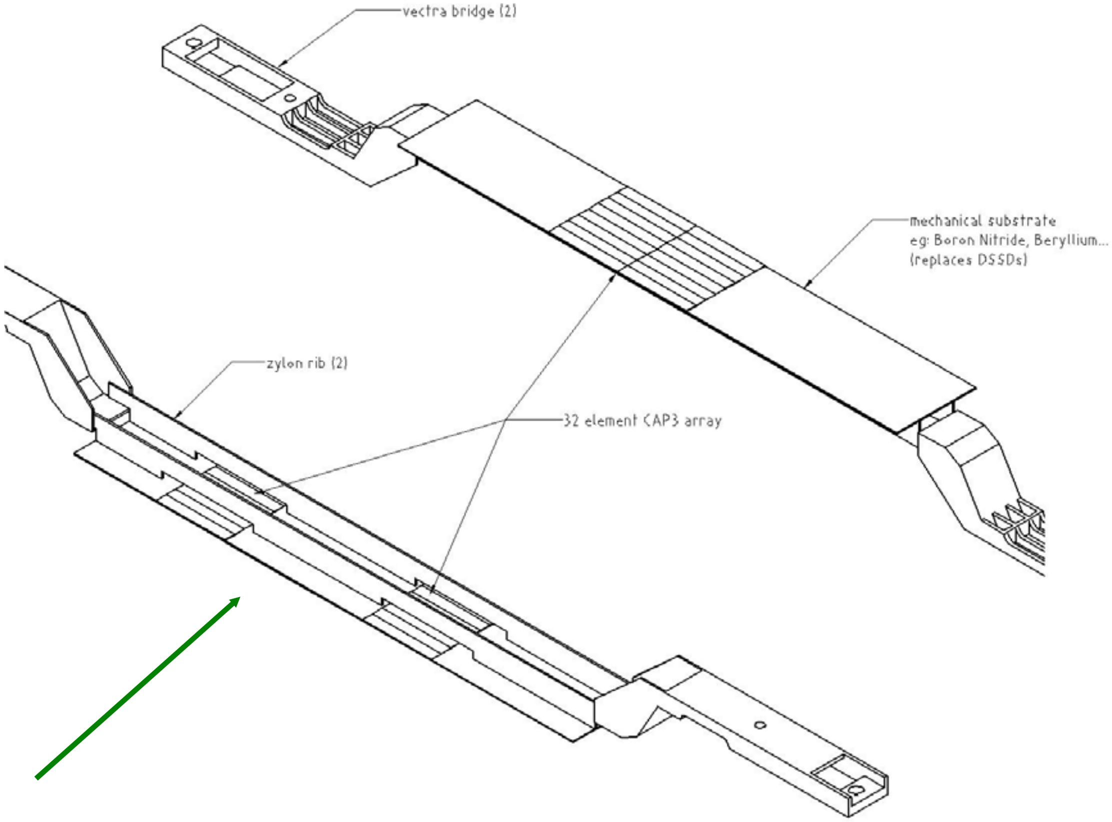


Reconfigured since last shown:
Started detailed mechanical design –
Marc Rosen

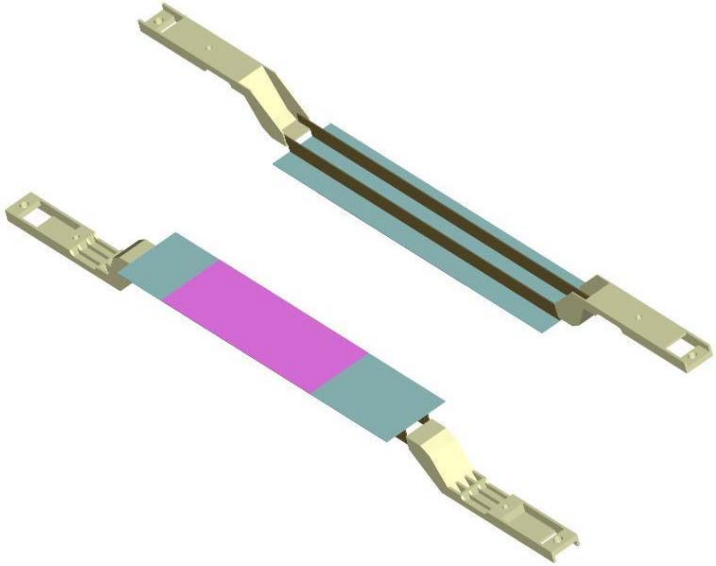


8 wide works

Short-term Upgrade (3)



4 x 8 CAP3 basically spans
Belle acceptance



32 CAP3/ladder

6 ladders/L1 layer

22.8 Mpixel "camera"

20-30kBytes/event (after L3)

Summary: Critical R&D Milestones

1. Readout Speed

100kHz frame rate, 10kHz L2 accept

10μs frame acquisition OK (CAP2), CAP3 to test 100μs frame readout

2. Radiation Hardness

>= 20MRad

Leakage current OK (CAP1), q collection efficiency TBD

3. Thin Detector

<= 50μm, double layer

50μm mechanical dummies, CAP3 to be thinned (SNF)

4. Full-sized detector

Span acceptance (reticle limit)

CAP3 fabricated – performance evaluation under way

Backup material

CAP3 DAQ

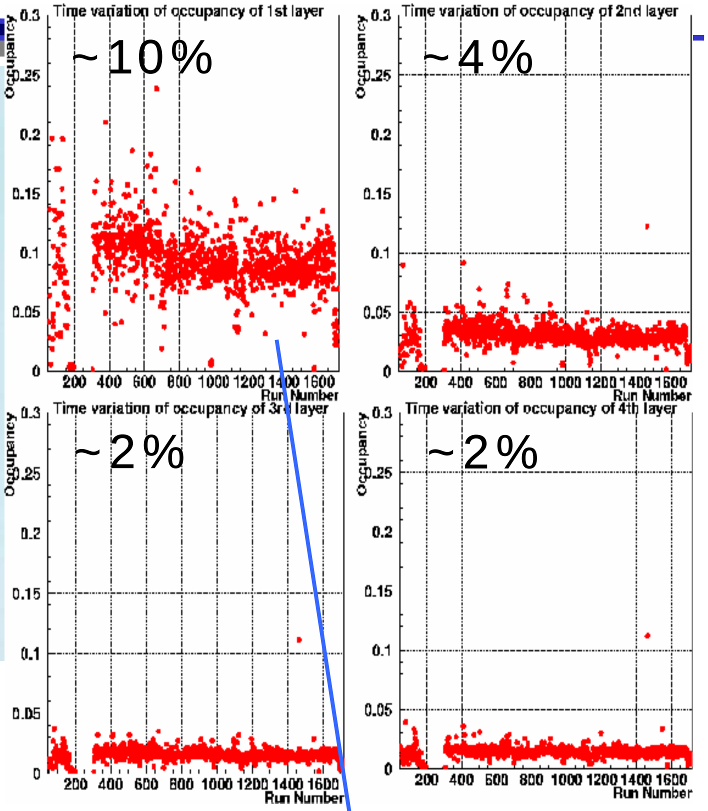
New CPU card for DAQ:

from a slow 300 MHz PIII processor for CAP1/CAP2

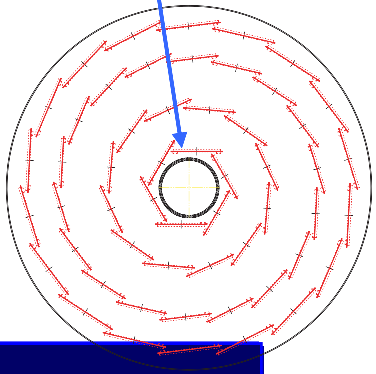
to 2.2 GHz Pentium4 and neat 2.5” 100Gb on-board disk (using Fedora Core 3)

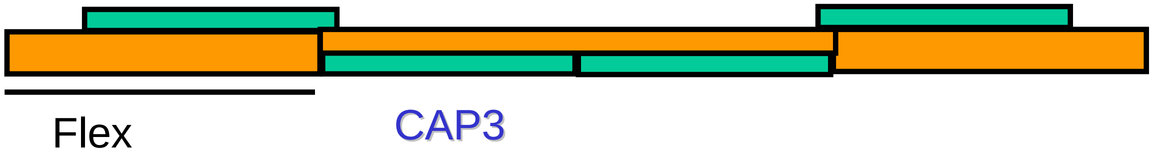
→improve the speed of data acquisition.

“Fast” Intermediate Belle SVD2 L1 upgrade option

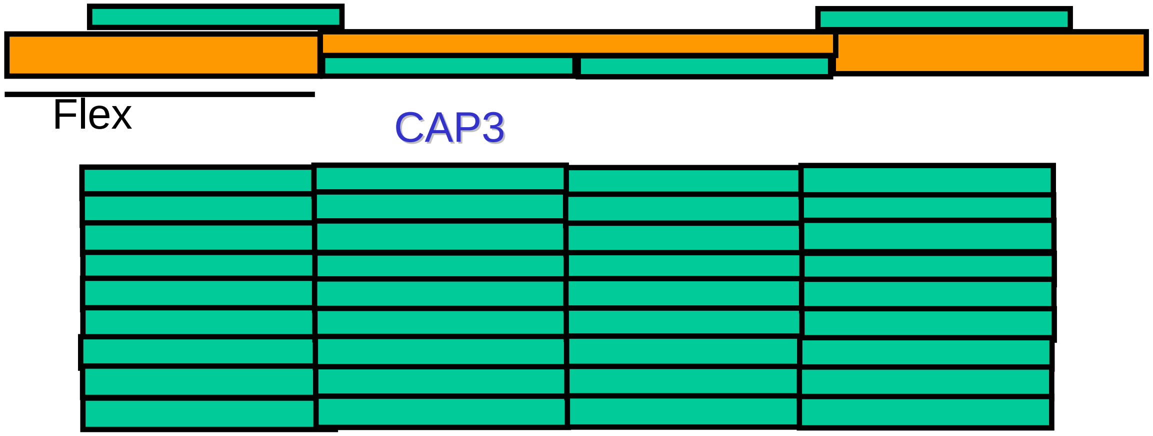


Replace Layer 1 with CAP3 pixels
Mechanically identical (drop in)





Belle SVD L1 upgrade



4 x 9 = 36 CAP3 / L1 ladder

6 ladders/L1 layer

~26M Channels total

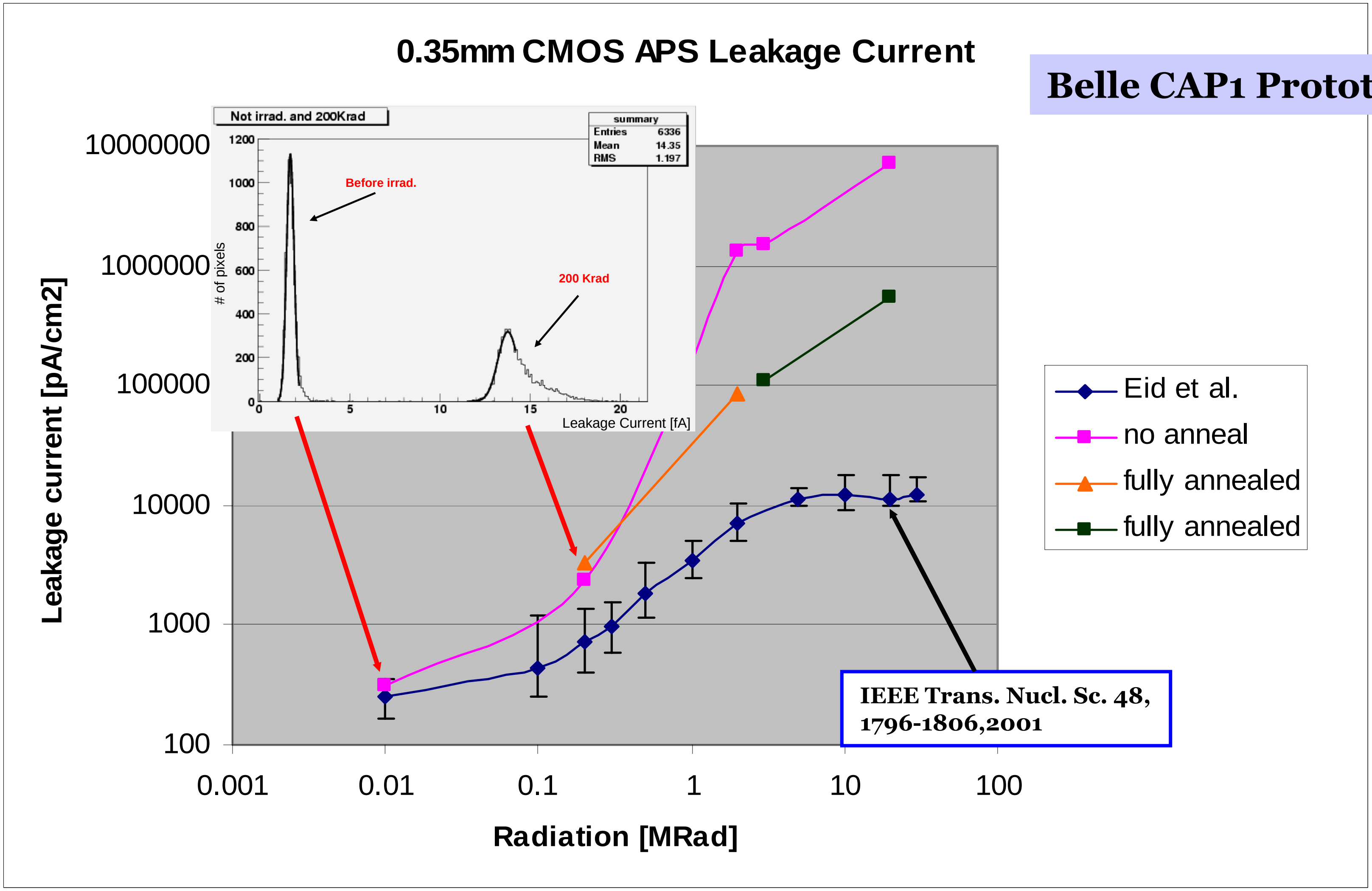
R=7mm configuration: 6.6M channels

SVD L1 * 40 background ~ few 100kBytes/event

➔With L3 SVX track match: ~few 10kBytes/event

Irradiation: leakage current

Belle CAP1 Prototype



IEEE Trans. Nucl. Sc. 48, 1796-1806,2001