Update from UH: Precision Timing and Continuous Acquisition Pixels

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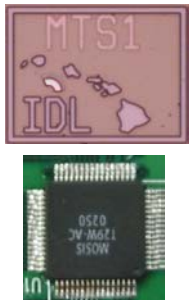
Mini-Trig/DAQ Workshop
November 2003
@Nara

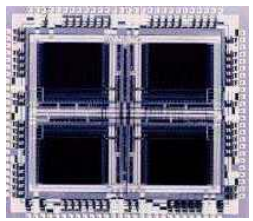
Precision Timing Update

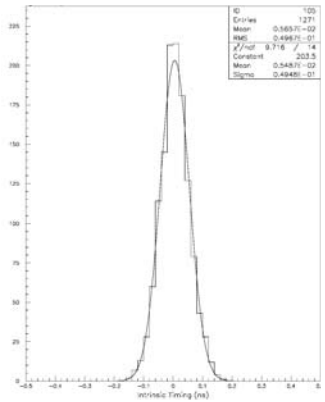
- Two viable techniques:



+

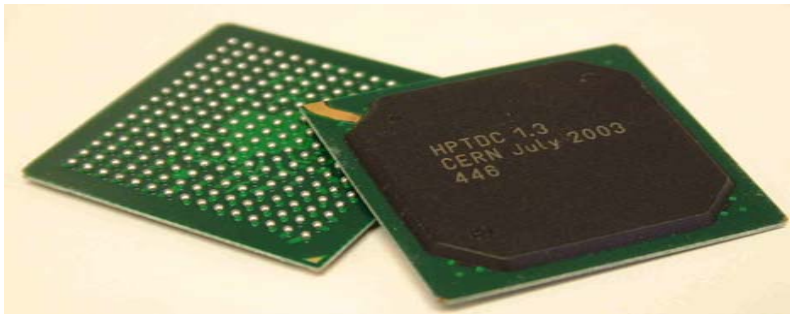
TMC



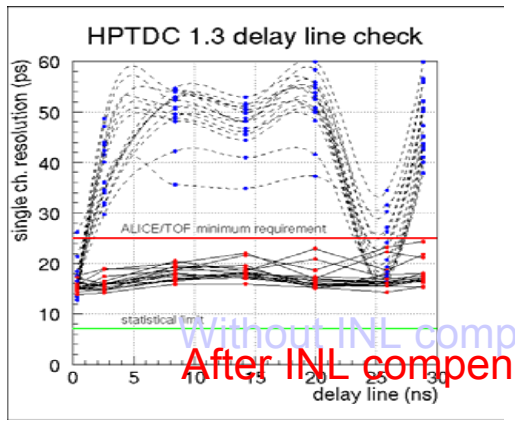


σ~ 25ps
(system subtracted)

Both require calibration for high precision performance



Measurements from ALICE-TOF



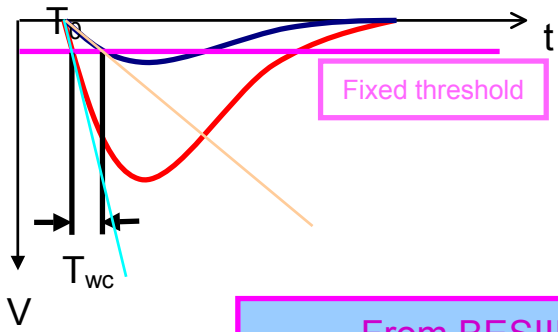
- Both options are possible
  - Cost benefit to HPTDC solution (<$8/channel)

TDC Comparison

- MTS + TMC Benefits:
  - We control the design
  - Separate TS and TDC clocks
- MTS + TMC Negatives:
  - 2 chips
  - More expensive
  - Less well tested (many users, CERN evaluation)
  - MTS1 must be ported (competing with pixel effort)
- HPTDC Negatives:
  - Production order “lifetime buy” in 2004
  - Still a few bugs
  - Complexity: many, many registers…

PID Concerns

- Concern about discriminators
- Our old nemesis, TWC
- Not tightly coupled to detector R&D
- No idea about barrel channel count



From BESIII Workshop June, 2002
Applies to high resolution TOF proposal

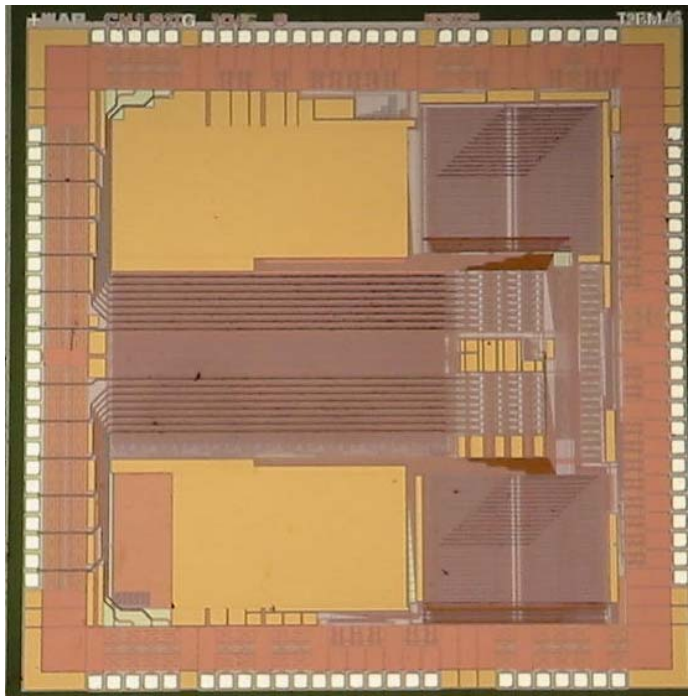
	Belle		BESIII		
	Spec.	guess?	Spec.		
RF/BCO	<35 ps	35 ps	<35 ps		
uncorrected t=0		?	?	within run	
Discrim. Overdrive		?	?	could be calibrated	
Beam bunch length	2.5 mm	8.3 ps	50 ps	15 mm	
Time Encoding	<20ps	22 ps	?		
		(~42 ps)			
TOTAL	< 40 ps	**~45 ps**	< 45 ps ?	looks difficult	

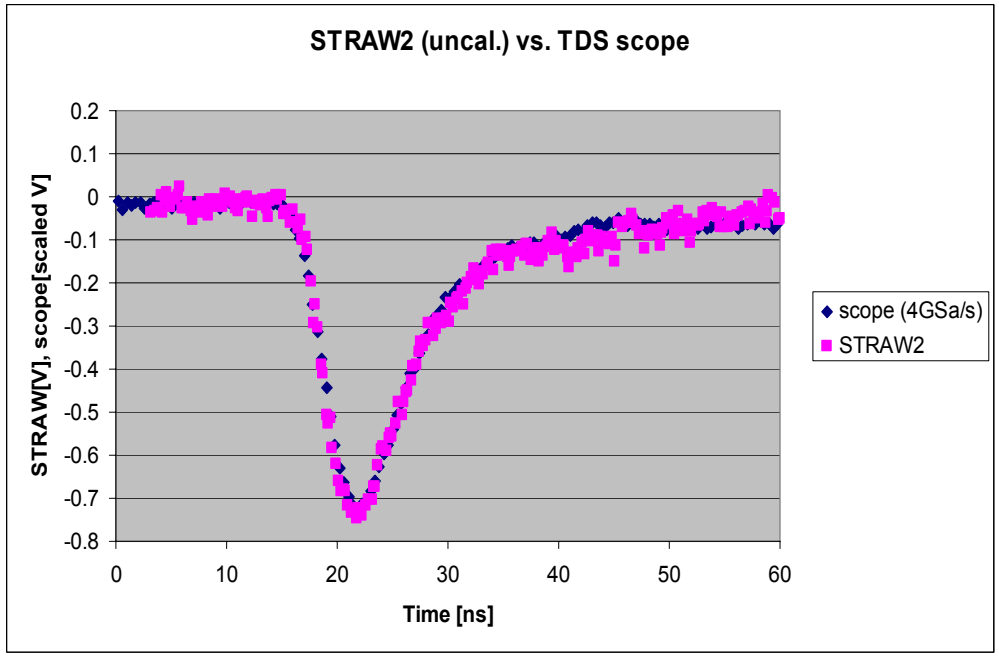
- GEANT/full simulator contribution:

σ^2_{fin} → 100ps – "known" ~ "physics" → 40ps

Waveform Sampling

- Looks very promising:





- GHz analog bandwidth, multi- GSa/s – depth issue
- Will keep in my back pocket…

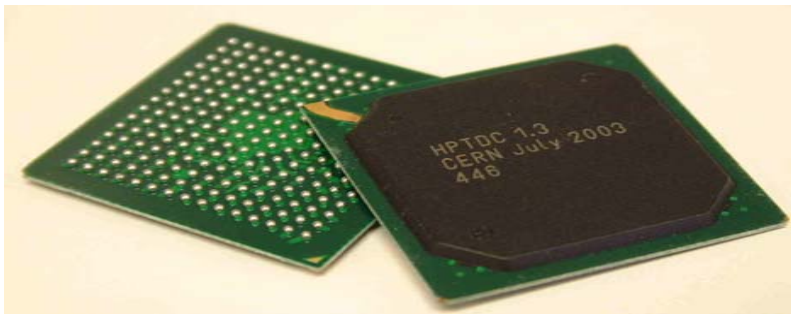
2004 FINESSE Efforts

- CuEval2

(Migrate to COPPER2)

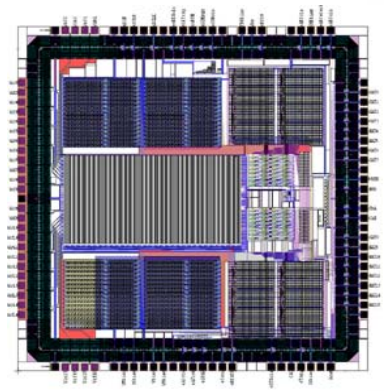
[Belle Note "soon"]

- HPTDC (10 samples)

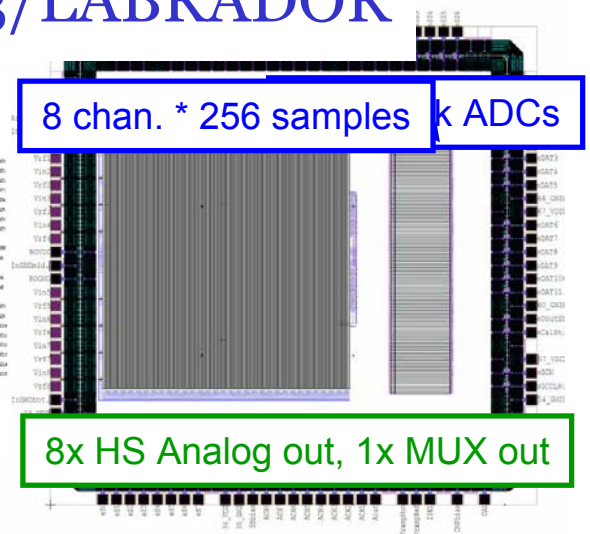


- Precise RF clock avail.?

- STRAW3/LABRADOR



STRAW3



- Need a stable COPPER

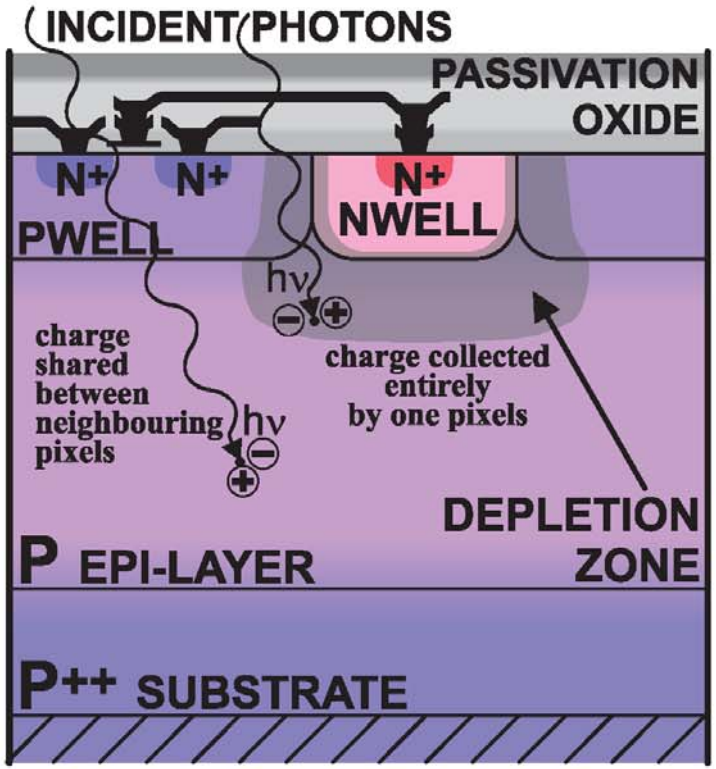
Momentum Toward APS upgrade

- There has been much Active Pixel Sensor progress recently:
  - LEPSI/TESLA(MIMOSA) & LBNL/STAR prototypes
    - Hawaii has been evaluating STAR prototype
    - RAL (APV25) also getting into the act
  - Hawaii is fabricating 2 protos (CAP1,CAP2) for B-factory
    - Will explain more about today
  - Beam test of Belle pixel proto sometime next year
  - For use in Belle/Super-Belle, some implications for DAQ
    - Maximum readout latency? (pipelined)
    - Trade-off of latency vs. compression
    - In the spirit of "adiabatic" improvements, we may not have to wait for Super-B shutdown to replace SVD2 L1 with pixels – but not if DAQ can't handle it

A Truly Attactive Proposition

CMOS Monolithic Active Pixel Sensors (MAPS) principle

"From digital cameras to particle tracking device"



-The active volume (epi-layer, ~10 µm thick) is underneath the readout electronics, providing 100% fill factor

-The charge generated by ionization is collected by the n-well/p-epi diode

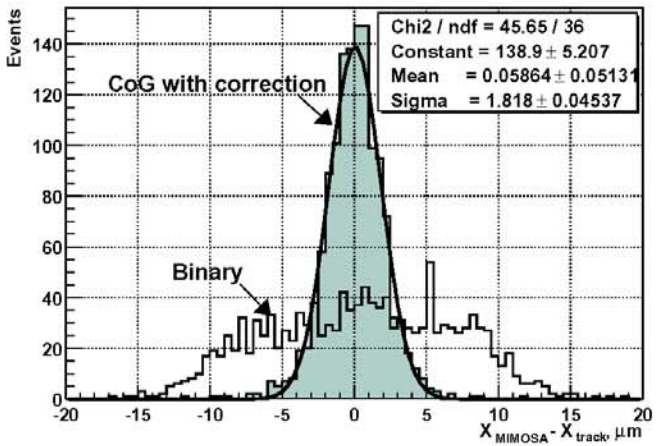
-Charge collection is achieved by the thermal diffusion

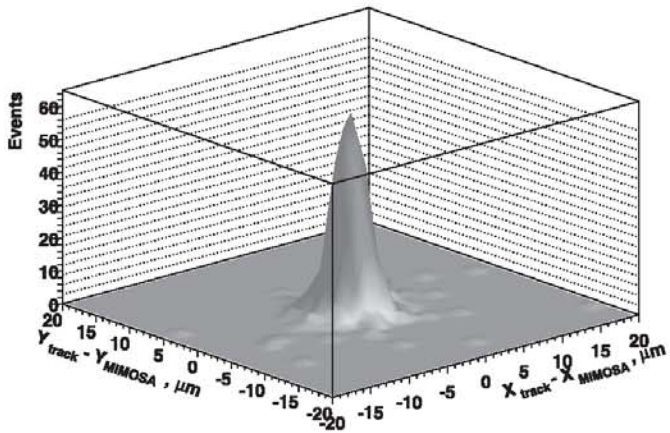
The device can be fabricated using a standard, cost effective and easily available twin-tub CMOS process on epi substrate. No post-processing (e.g. bump-bonding)!

System-on a chip approach possible

Promising Results

CMOS MAPS particle tracking performance (20 µm pitch)





ENC ~10 electrons: S/N>30

Efficiency (5σ seed cut): ε_{MIP} > 99 %

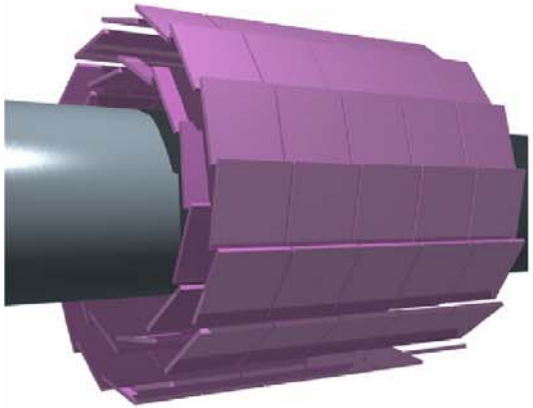
Spatial resolution: σ = 1.4 µm

Demonstrated on several devices in various submicron CMOS processes:

AMS 0.6 µm, 14 µm epi
Alcatel 0.35 µm, 4 µm api
AMS 0.35 µm, no(!) epi
…
TSMC 0.25 µm, 8 µm epi
(LBL team)

+UH, RAL

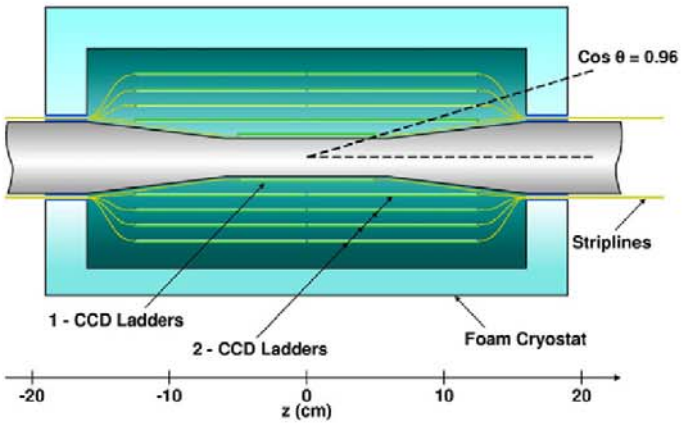
Other Experiments Considering



STAR μvertex detector

1. First upgrade (x4 present luminosity, 2006):
   10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008):
   2 – 5 ms readout (integration) time

Super-Belle: 10μs ?



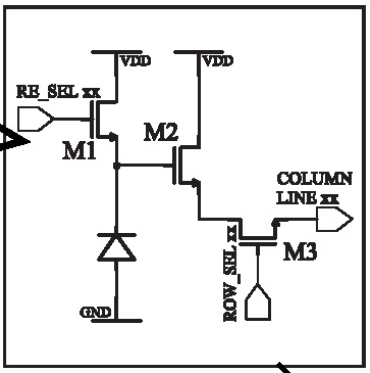
TESLA Vertex Detector*

1. Outer layers readout time: 100 -200 μs
2. Innermost layer readout time: 25 -50 μs

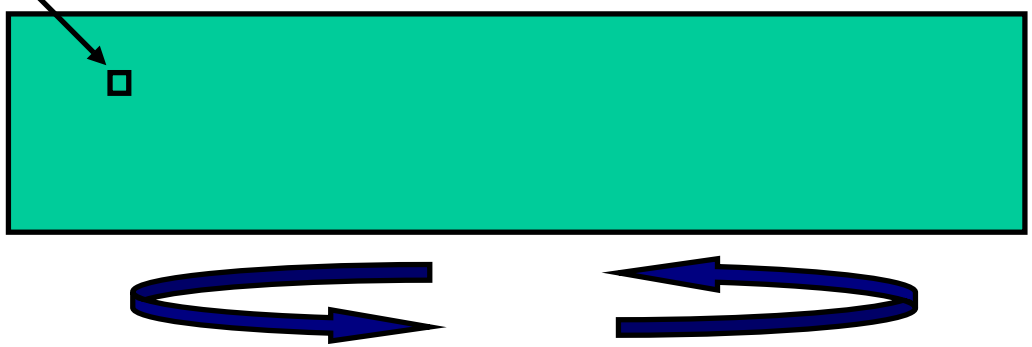
*NLC/JLC: t~10 ms

Continuous Acquisition Pixel

- Conceptually Simple
  - Analog reset, sample & then sample continuously
  - Row-wise analog shift out as fast as possible:
    - Consider 22.5μm pitch output w/ 4:1 AMUX
    - 100MSa/s output (e.g. 8-bit ADC on output)
    - 10μs for 1k columns (# row independent)
    - Possibility of passing signals through to allow joining to form ladders



Standard APS pixel



Pixel Array: Column select – ganged row read

High-speed

analog

ADC

& storage

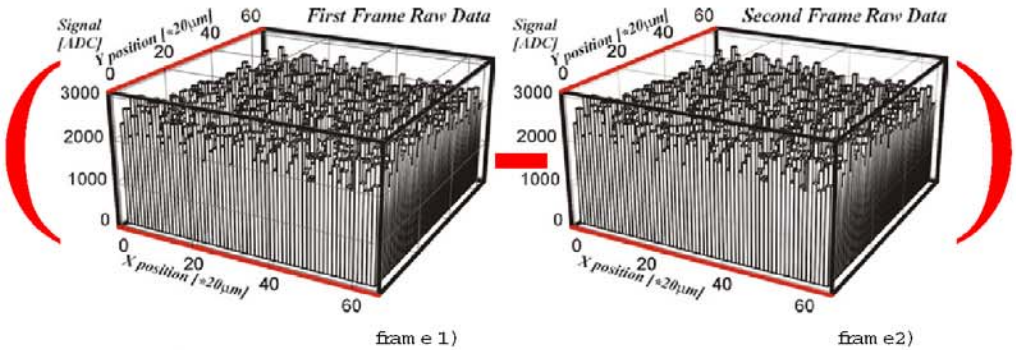
Low power – only significant draw at readout edge

CAP1 Concept

- Automatic CDS
  - When receive L1 trigger:
    * sift data in sync pipe and provide the difference in value for orbit with trigger and preceding orbit
  - Analog reset
    - If can reset once every 100 orbits, 1% "deadtime"
    - 1μs "reset" and 10μs to obtain a baseline sample
    - Possibly even less, depending upon dynamic range and background
    - Can build "intelligence" into reset
      - When starting to saturate
      - L1 busy
    - Minimization of leakage current important
    - Relatively simple to fabricate

Correlated Double Sampling

Data processing: (Digital) Correlated Double Sampling

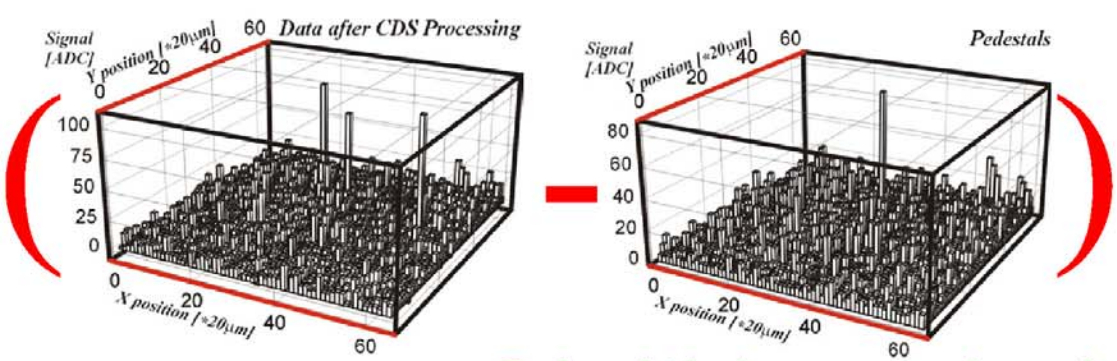


Useful signal on top of Fixed Pattern DC level

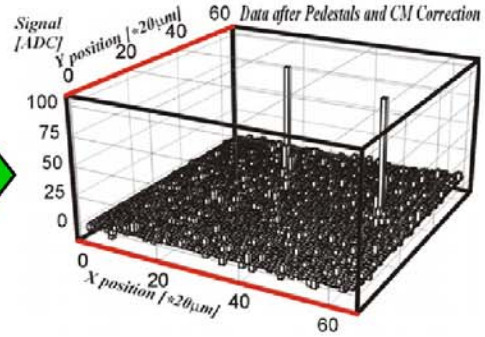
Fixed Pattern dispersion: ~100 mV

Typical signal amplitude: ~1mV

(frame2 - frame1) subtraction



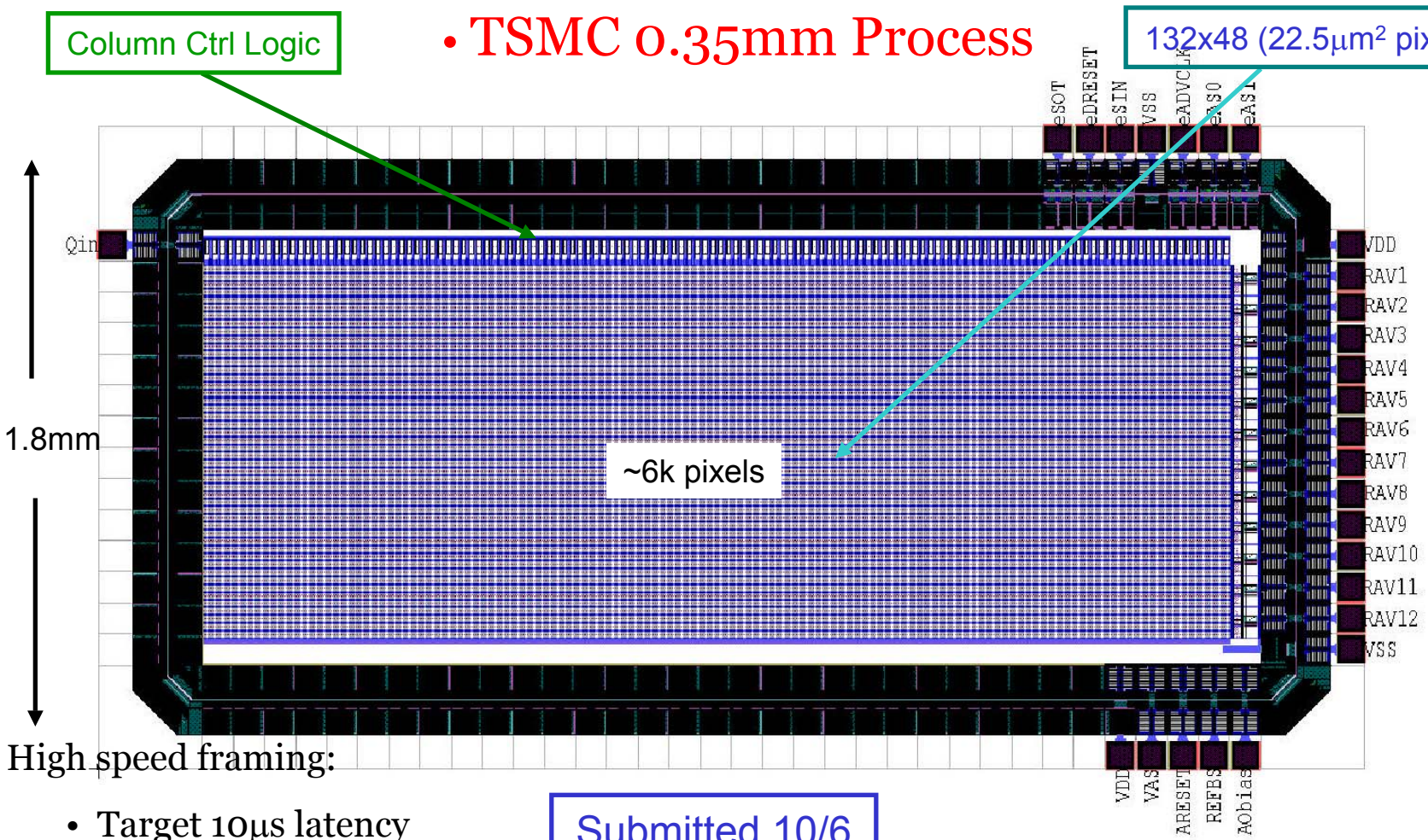
Pedestal (dark current) subtraction



Hit candidates!

CAP1 Prototype

- TSMC 0.35mm Process



- High speed framing:
  - Target 10μs latency
- Pipelined readout

Submitted 10/6
Due back 12/10

"slow" RO resolution ~ 2μm

CAP2 Concept

- CAP1 architecture difficulties:
  - Significant strain on analog output transfer:
    * 10ns settling time difficult (will test, but SPICE simulation shows marginal for full-sized detector)
  - Data volume reduction
    - Better if can provide true on-detector pipelining
    - Reduce power if constrict data flow to L1/L2 accepted events (100kHz→ 10kHz or 1kHz):

    40GSa/s → 4GSa/s or 0.4GSa/s

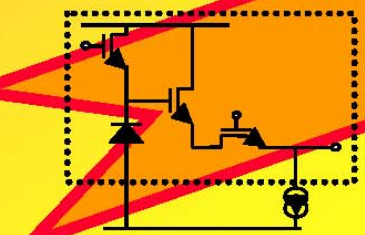
Possible to put a small pipeline in each pixel?

Yes! In fact not unique (RAL)

From PPARC Funding proposal request

Design for science-grade MAPS

Where we come from



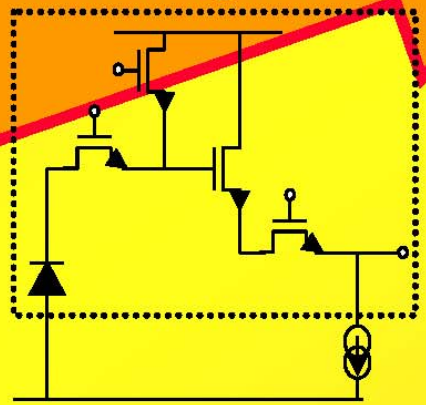
Consumer MAPS.

3 transistors

Simple, but high noise, no data processing, …

Where we went from 2001 till now

1st science-grade MAPS

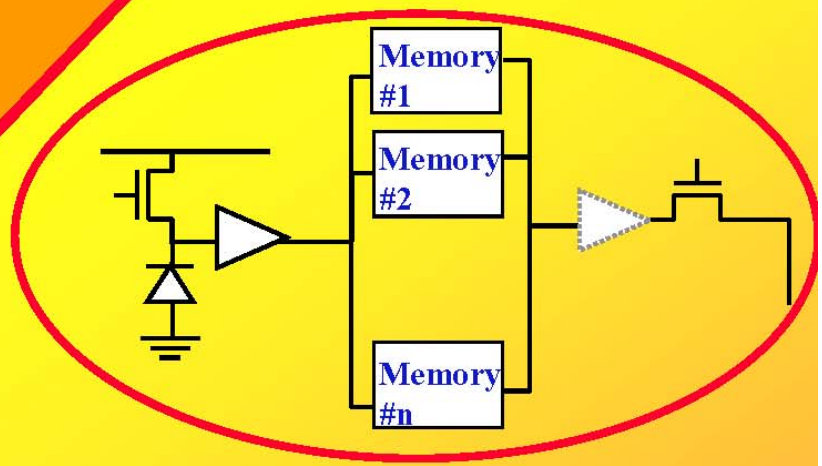


4 transistors

Reduce kTC and fixed pattern noise, but still relatively slow and no data processing

Where we want to go

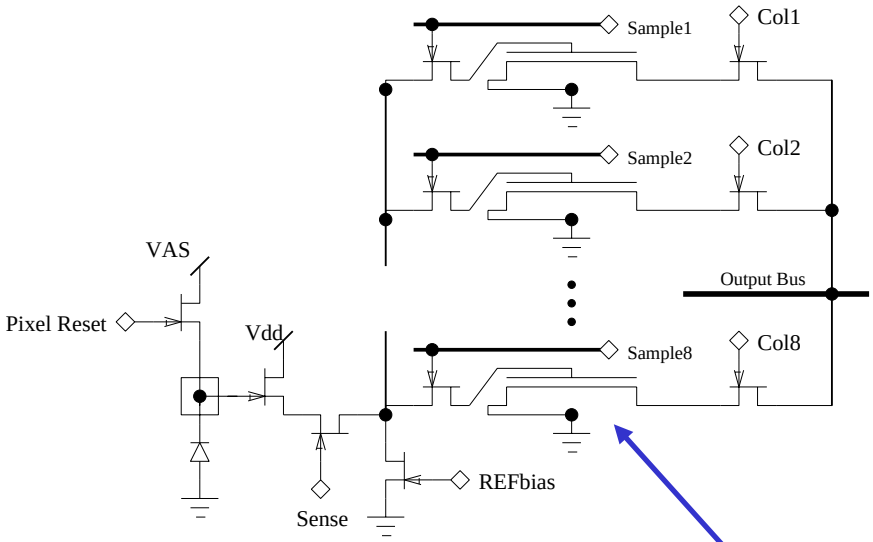
Flexible Active Pixel Sensors

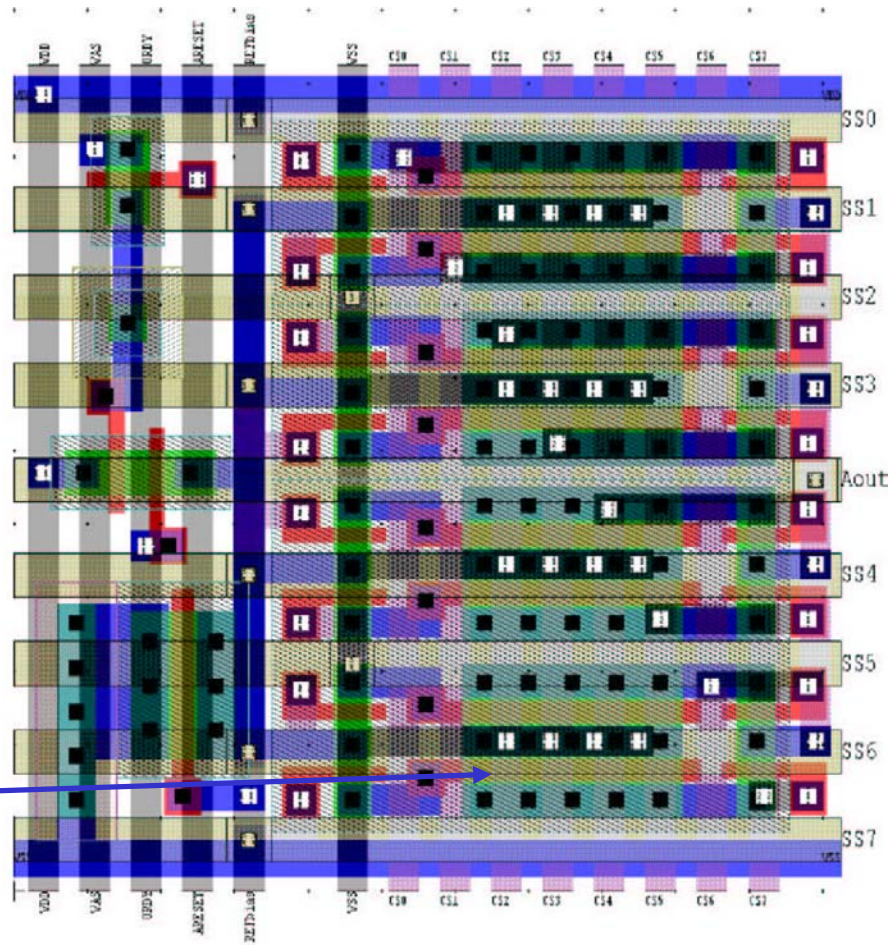


8 transistors + memory cells with storage and selection transistor

Very high speed, analogue data processing, reduced noise, necessary for particle physics applications

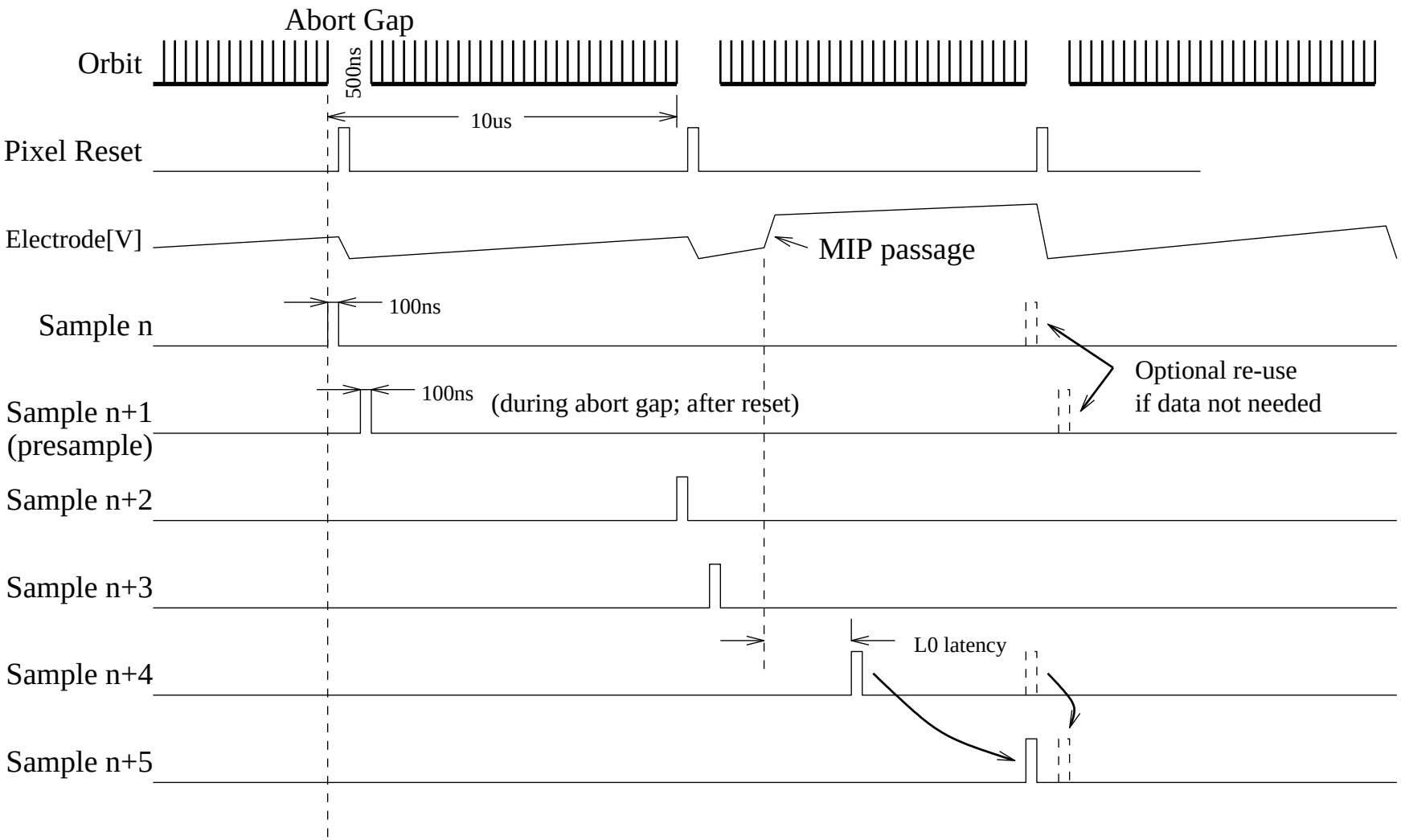
Octal-pipeline (in 22.5μm² pixel)





Storage cell

One Operating Mode

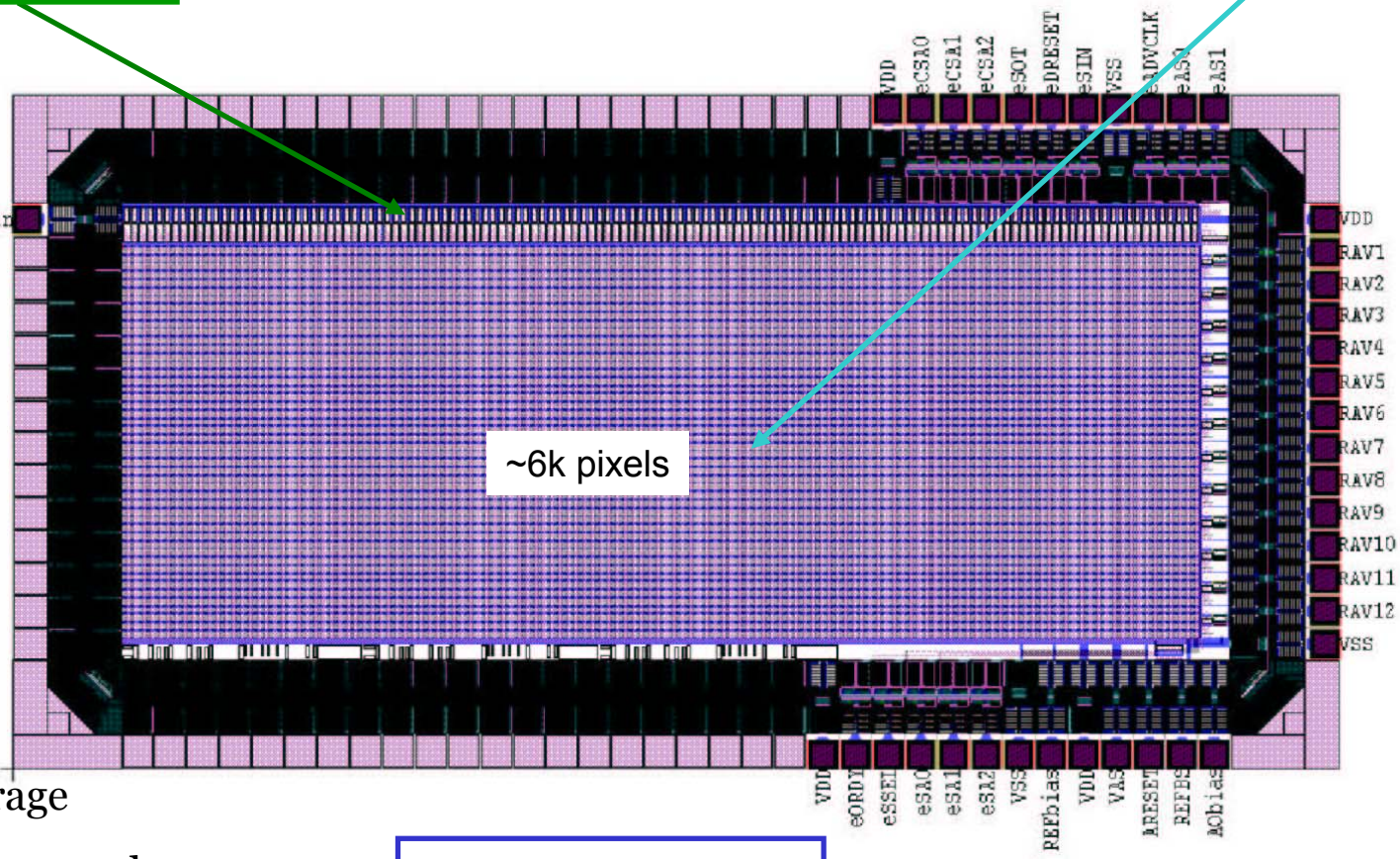


CAP2 Prototype

Column Ctrl Logic

• TSMC 0.35mm Process

132x48 (22.5μm² pixels)



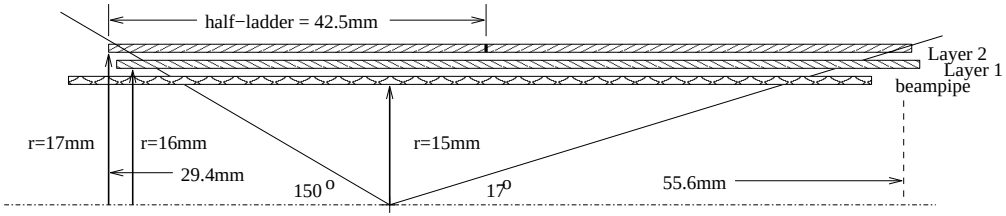
1.8mm

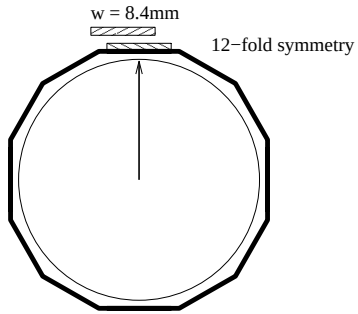
- 8-deep storage
  - Target 50μs latency
- Triggered readout

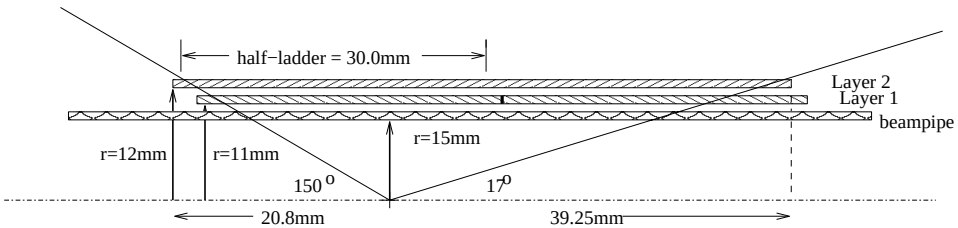
Submitted 10/27
Due back Jan 10?

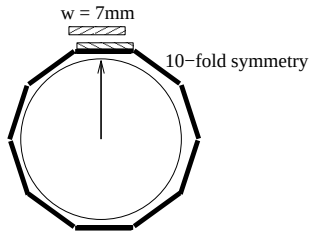
"slow" RO resolution ~ 2μm

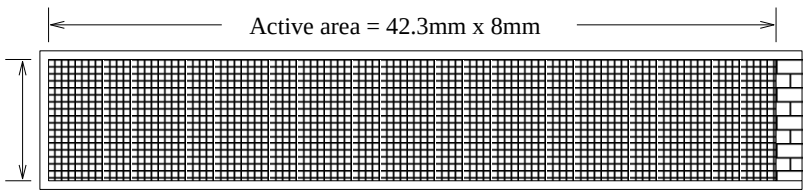
Channel Count







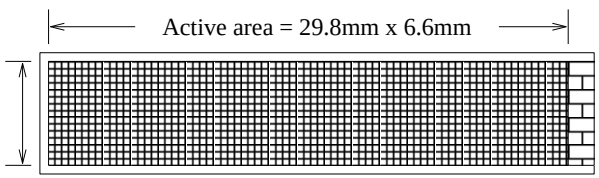




1880 x 356 = 669k channels

2 layers * 24 HL = 32M pixels

Half-ladders:



1324 x 293 = 388k channels

2 layers * 20 HL = 15.5M pixels

Required Transfer Rates

- CAP1 architecture (if 10μs max. latency):
  - 15mm radius:
    - 67 Gpixels/s
    - ~1Gpixel/s/pin
  - 10mm radius
    - 39 Gpixels/s
    - ~0.5Gpixel/s/pin
- CAP2 architecture (>= 100μs max. latency):
  - 15mm radius:
    - 6.7 Gpixels/s
    - ~100Mpixel/s/pin
  - 10mm radius
    - 3.9 Gpixels/s
    - ~50Mpixel/s/pin

Two ways around:
Multi-orbit
"Tiling"

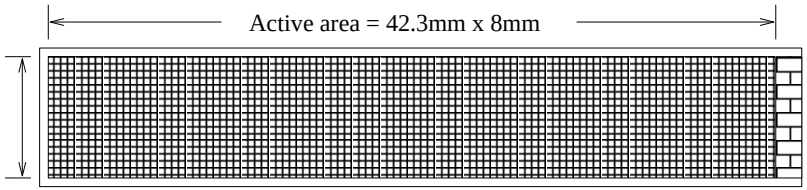
Real max. latency
Set by <L1/L2> rate

Occupancy Scaling

- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm²
  - Pixel spatial reduction:
    - Pixel area = 22.5μm x 22.5μm = 506 μm²
    - Reduction factor ~8400
  - Pixel temporal loss:
    - 0.5μs SVD vs. 10μs PVD (could be improved)
    - Increase factor ~ 20
  - Grand total:
    - 10% * 20 * 8400^{-1} * 20
    - Can expect ~ 0.5% occupancy

Event size

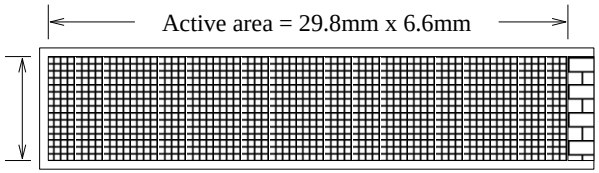
- Conservatively take 1% as Occupancy



1880 x 356 = 669k channels

2 layers * 24 HL = 32M pixels

320k Pixels



1324 x 293 = 388k channels

2 layers * 20 HL = 15.5M pixels

155k Pixels

- 1 Byte/pixel (8bit ADC) sufficient
- However, need ~25 bits of address info
- 4 Bytes/pixel → 620-1280kB/event
- Can reduce with clustering/track matching?

The Bottleneck

- Not trivial, but probably possible to:
  - Sample with adequate SNR
  - Read data off pixel with small enough latency
  - Provide periodic analog resets without incurring deadtime
- However:
  - Not easy to get this torrent to the electronics hut
    - Exploring 2 different fiber optics schemes
    - Custom SiGe mixer/modulator may be a solution
- Looks like can fit everything in one COPPER crate:
  - 1 high-speed fiber/half ladder
  - 1 high-speed fiber/FINESSE
  - Each FINESSE does all CDS/offset calculations
  - CPU does clustering?

"Kiseru"?

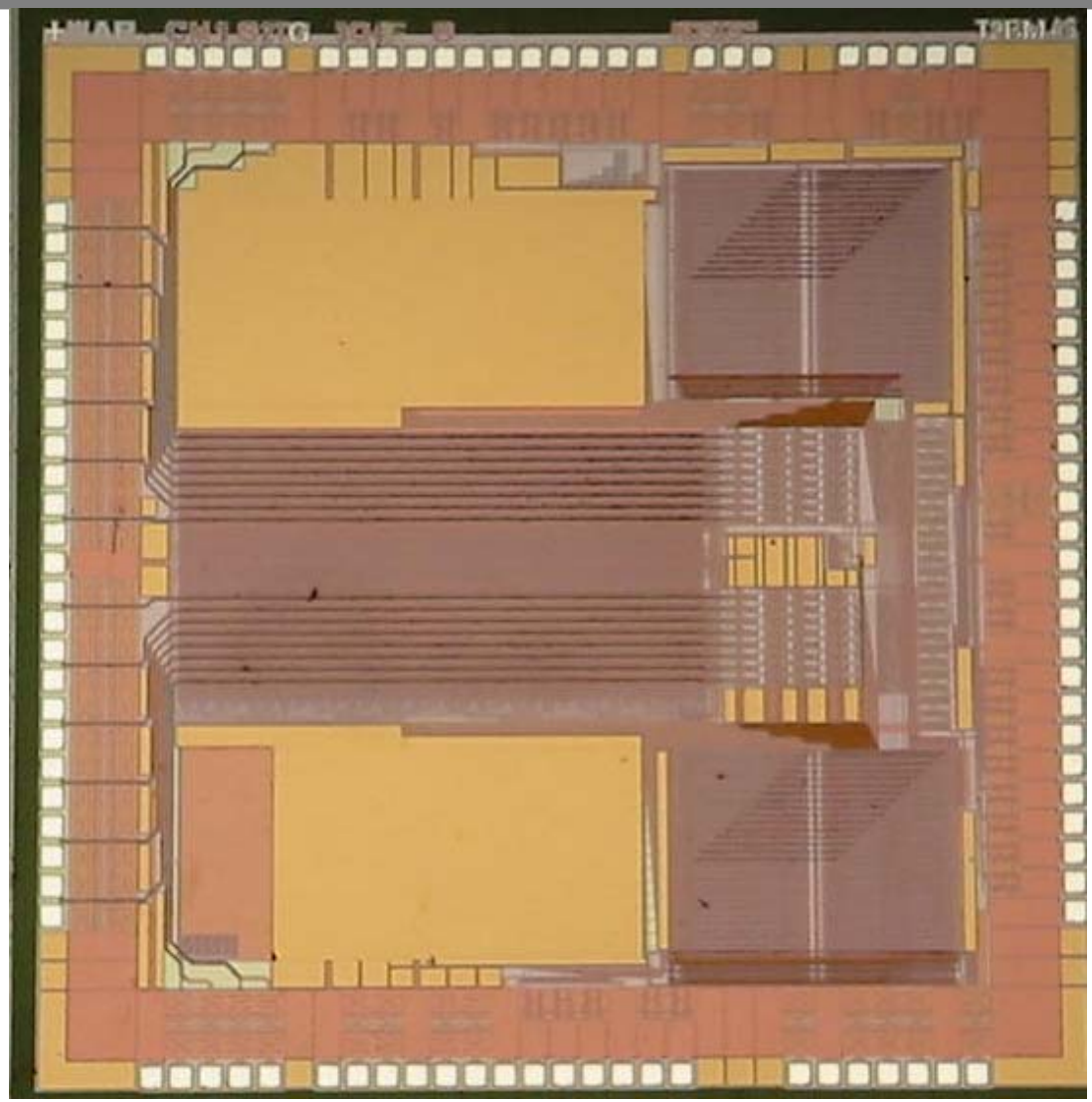
Summary

- Expect serious COPPER work to begin in 2004:
  - 3x FINESSE designs – one of which for *at speed* emulation
  - PID readout prototype electronics?
  - Settle system control issues
- Pixel Plans:
  - 2x prototypes in fab, full-size in 2004 (after beam test)
  - Much effort required on back-end
    - Enormous data volumes
    - Extreme bandwidth
  - Large reduction possible – algorithms?
- Items want to bring up while in Nara:
  - What really sets the max. latency?
  - Any useful pixel info at upper (L3/L4) level?
  - Next discussion: (next slide)

Super B Factory Workshop in Hawaii

January 19-22, 2004
East-west Center, Honolulu

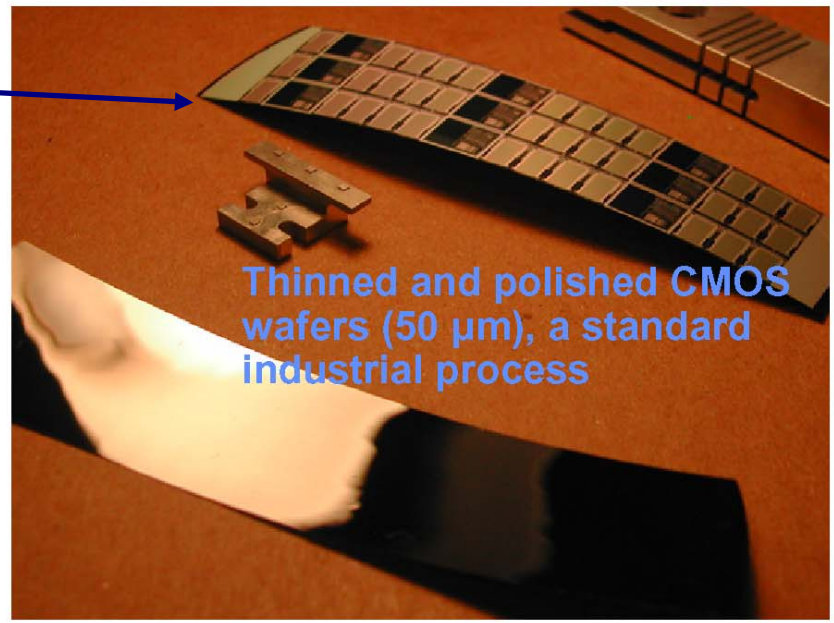
Back-up slides



Thin is In

1. **Thinning the substrate to 50 µm (or less)**
2. **Low mass (air?) cooling: keeping down the power dissipation (~100 mW/cm^2)**

LBNL old wafer

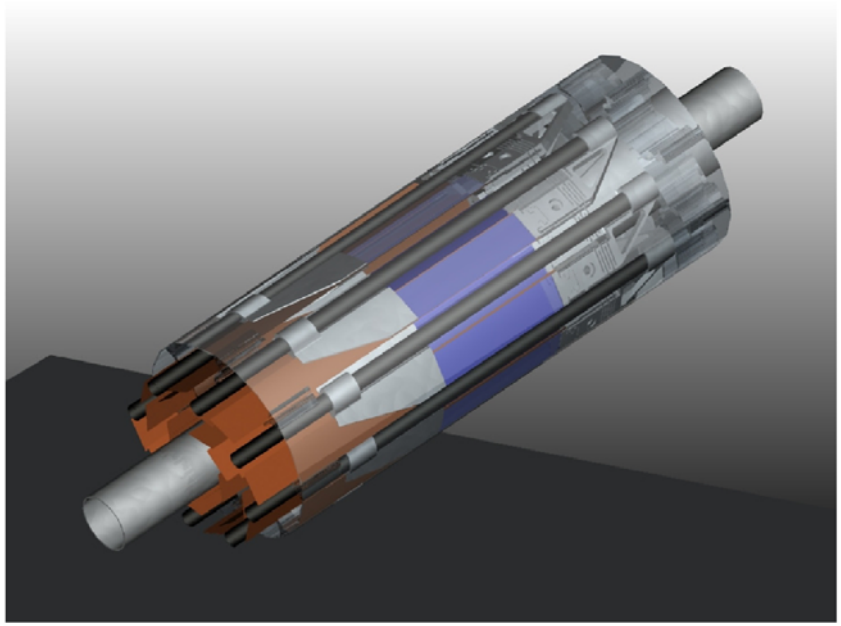


Sample 100µm Thick wafers from Chris Kenney

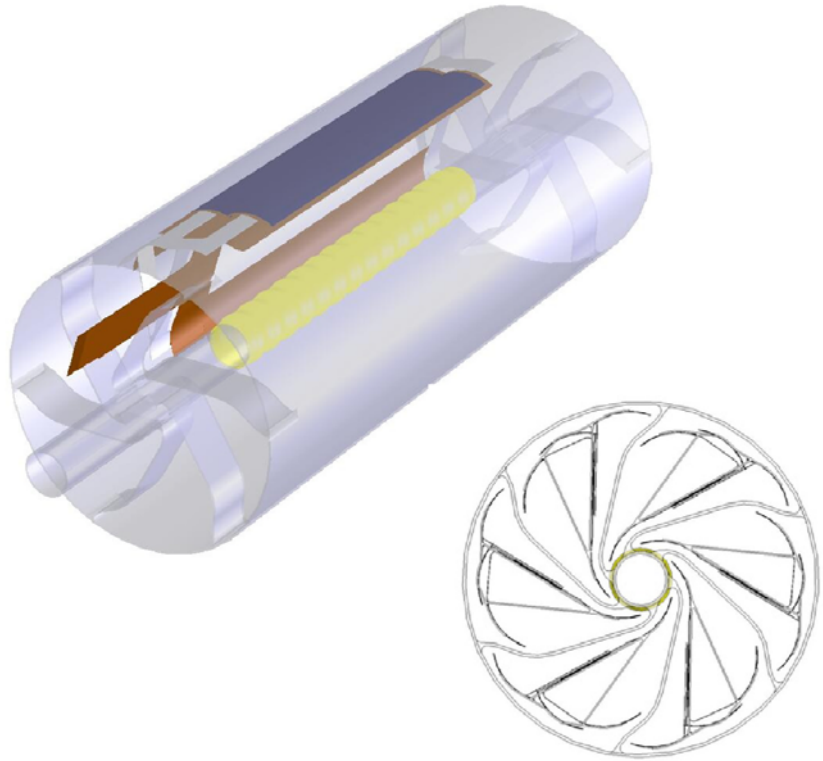
Mechanics

Very preliminary

Mechanical concepts of STAR Micro vertex upgrade using ultra-thin CMOS MAPS *



Tension concept



Self supporting Venetian blade concept

* Curtsey to Howard Wieman, LBL, STAR group

Marc Rosen has some ideas