

# Monolithic Active Pixel Sensors: Recent Progress

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for the Belle Pixel Group

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*KEK, Krakow INP, Univ. of Hawaii, Tsukuba Univ.*

Hiroshima STD 5



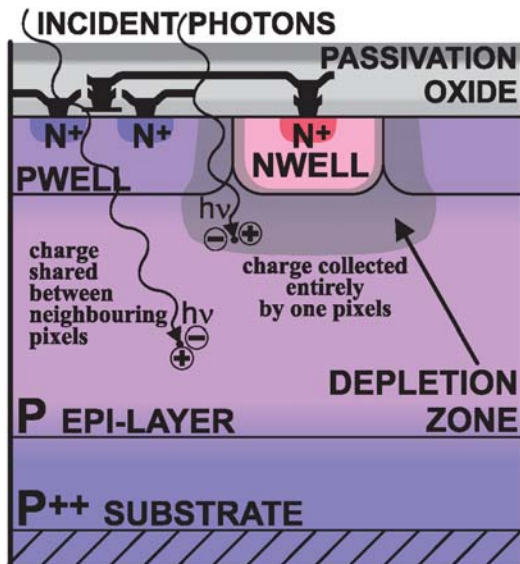
*R&D for Belle SVD*

*Upgrades*

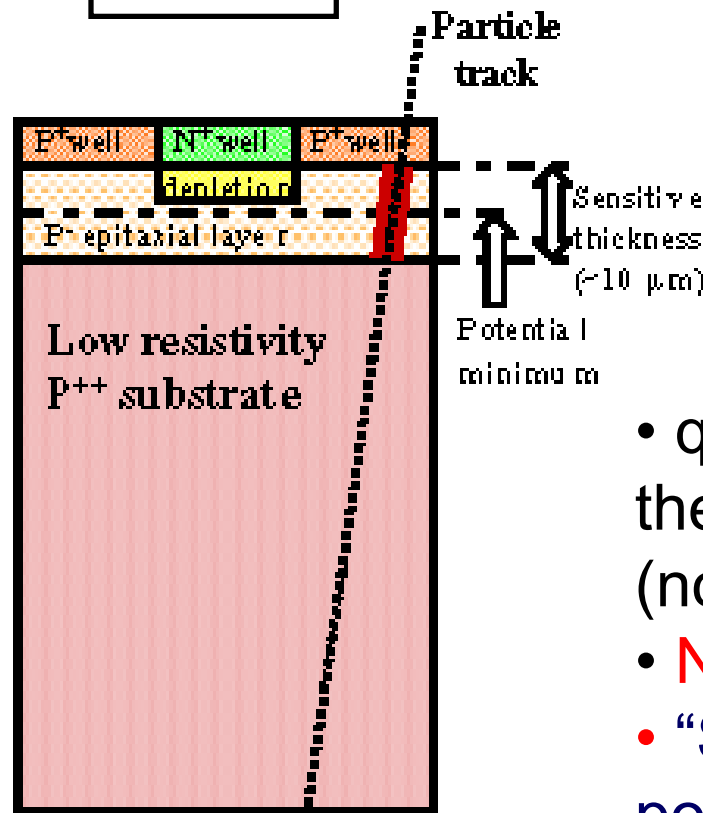
R=1cm / L $\geq$ 3x10<sup>35</sup>

# Basic Technology: Standard CMOS

CMOS Camera



Particle Detector



## Standard CMOS:

- Low Power
- Excellent Transistors
- Tight Process Control
- Excellent Uniformity
- High volume, low cost
- Large ADC, DSP base

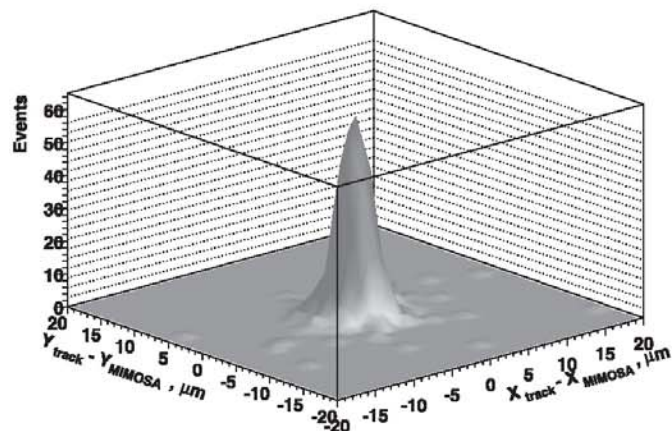
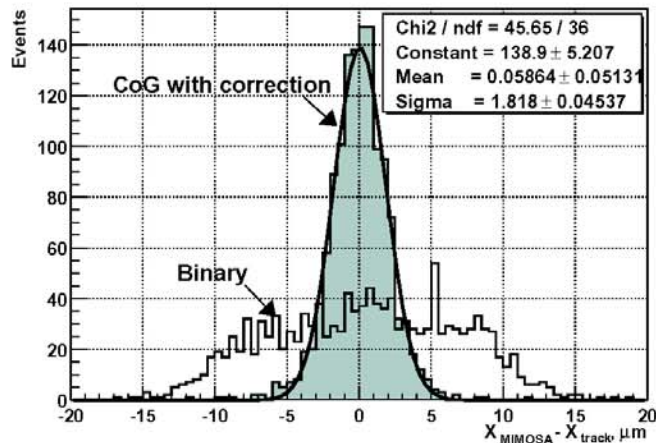
## Key Features:

- q collection via thermal diffusion (no HV)
- **NO bump bonding**
- “System on Chip” possible

Because of large Capacitance, need Thick DSSDs  
-- APS can be VERY Thin

# Promising Results

## CMOS MAPS particle tracking performance (20 $\mu\text{m}$ pitch)



**ENC ~10 electrons:  $S/N > 30$**   
**Efficiency (5 $\sigma$  seed cut):  $\epsilon_{\text{MIP}} > 99\%$**   
**Spatial resolution:  $\sigma = 1.4 \mu\text{m}$**

**Demonstrated on several devices in various submicron CMOS processes:**

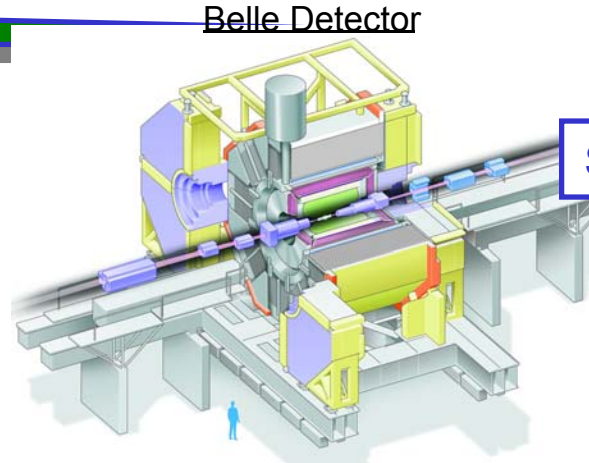
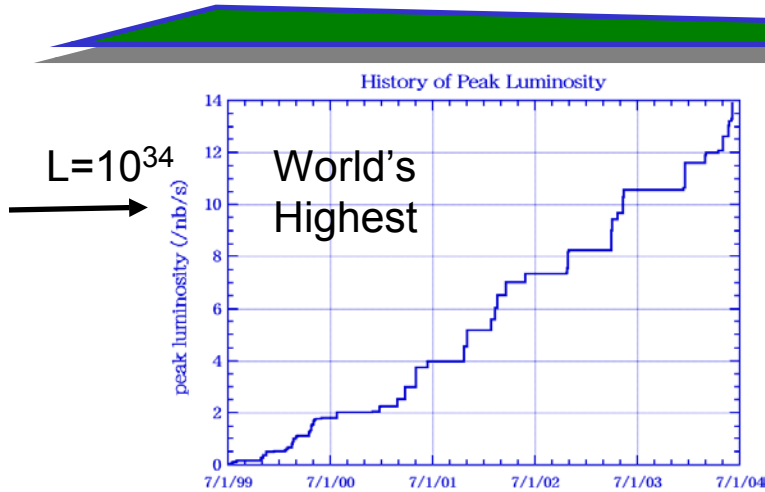
**AMS 0.6  $\mu\text{m}$ , 14  $\mu\text{m}$  epi**  
**Alcatel 0.35  $\mu\text{m}$ , 4  $\mu\text{m}$  api**  
**AMS 0.35  $\mu\text{m}$ , no(!) epi**

...

**TSMC 0.25  $\mu\text{m}$ , 8  $\mu\text{m}$  epi**  
**(LBL team)**

+UH,  
RAL,  
...

# Development Efforts



Super-Belle:  $\leq 10\mu\text{s}$

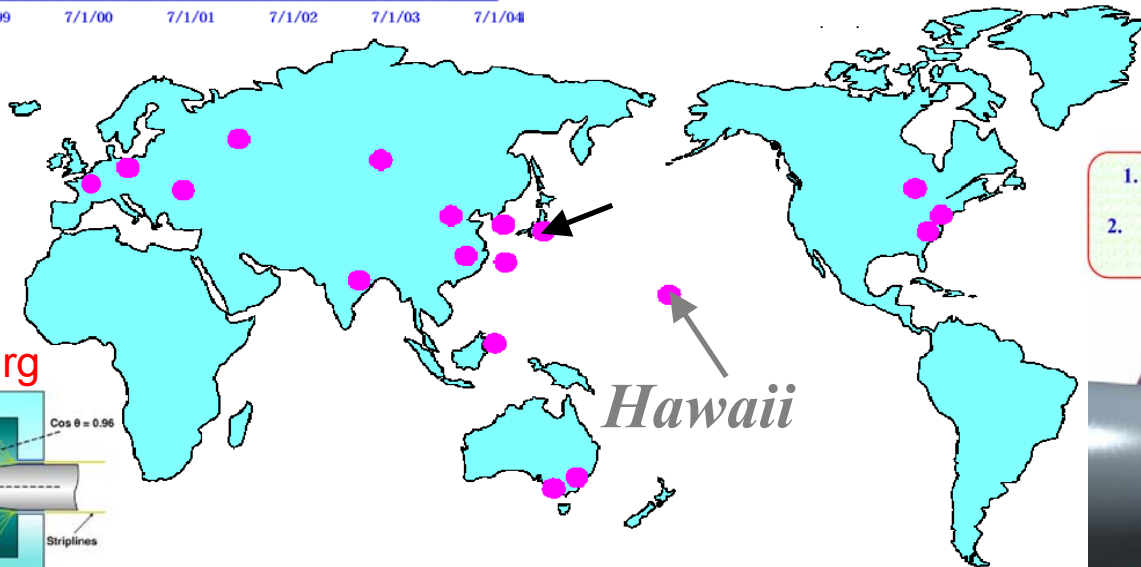
See T. Tsuboyama's talk

LBLN,  
UC Irvine

LEPSI,  
RAL,  
Strasbourg

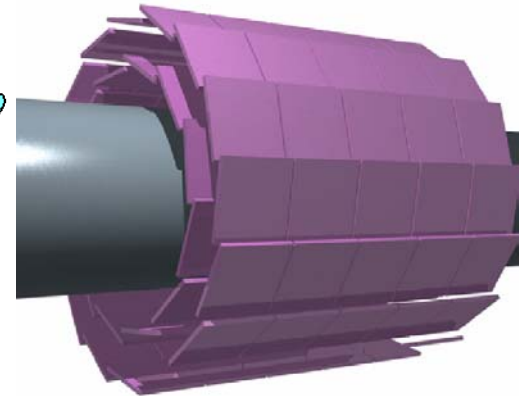
Linear  
Collider

DESY/Hamburg

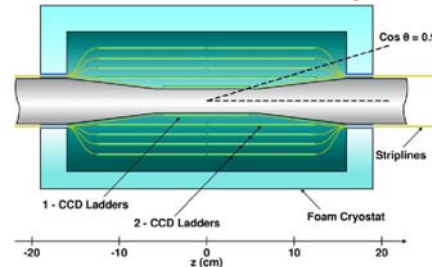


STAR  $\mu$ vertex detector

1. First upgrade (x4 present luminosity, 2006):  
10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008):  
2 – 5 ms readout (integration) time



Apologies to those not mentioned:  
Easy access will bring others

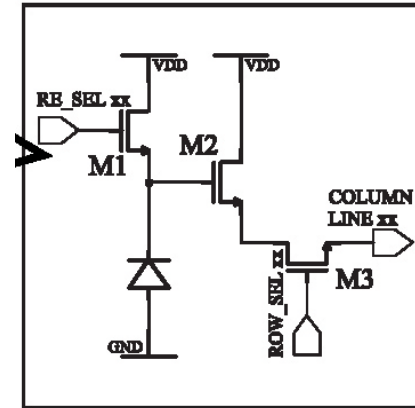
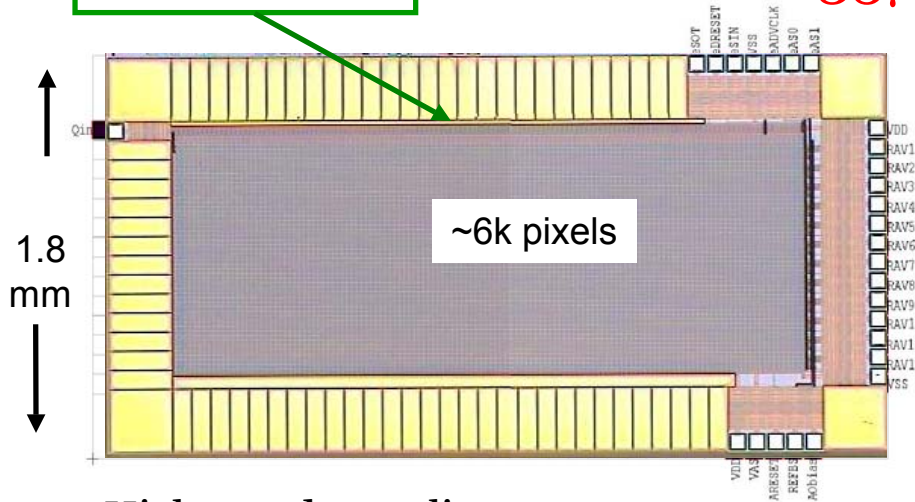


# Cont. Acq. Pixels (CAP) 1/2 Prototypes

Column Ctrl Logic

• TSMC 0.35 $\mu$ m Process

• CAP1: simple 3-transistor cell



• High speed sampling:

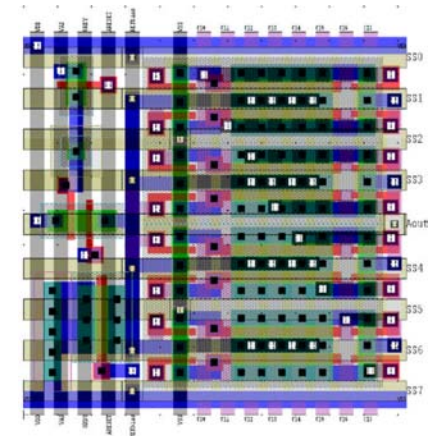
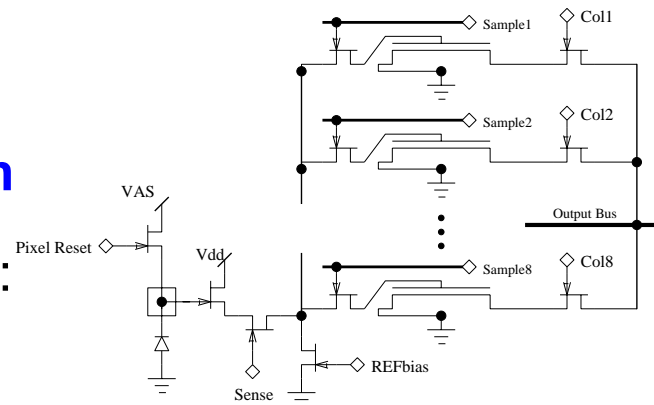
- Explore 10 $\mu$ s latency (CAP1)
- pipeline sampling(CAP2)

• CAP2: 8x mini-pipeline in each cell

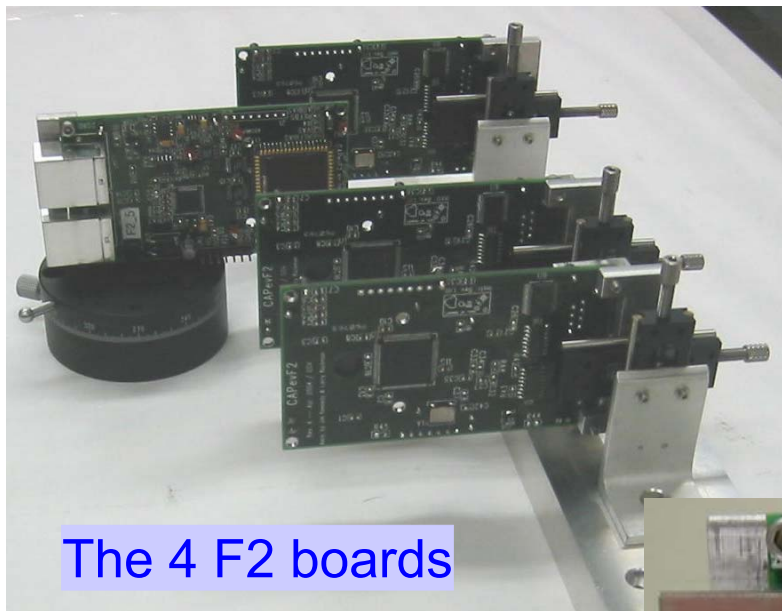
Pixel size: **22.5  $\mu$ m X 22.5  $\mu$ m**

Sample of CAP1/CAP2 tested:

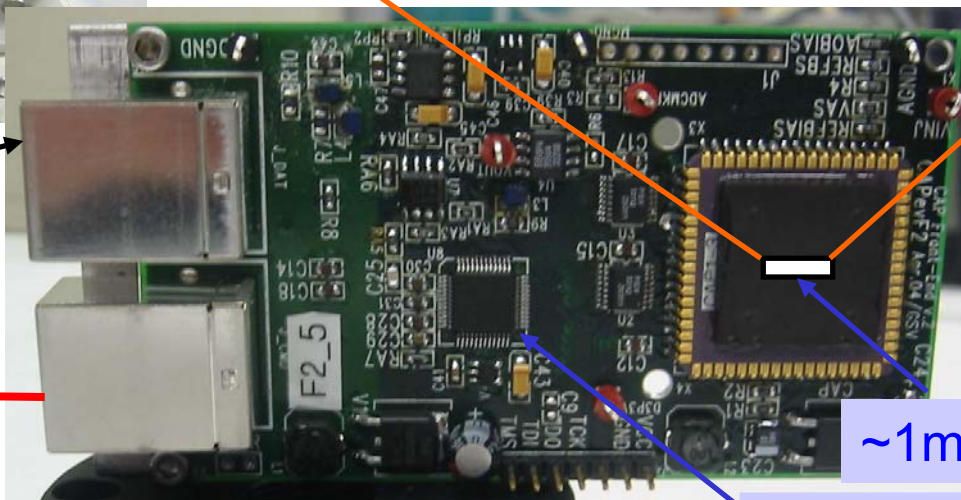
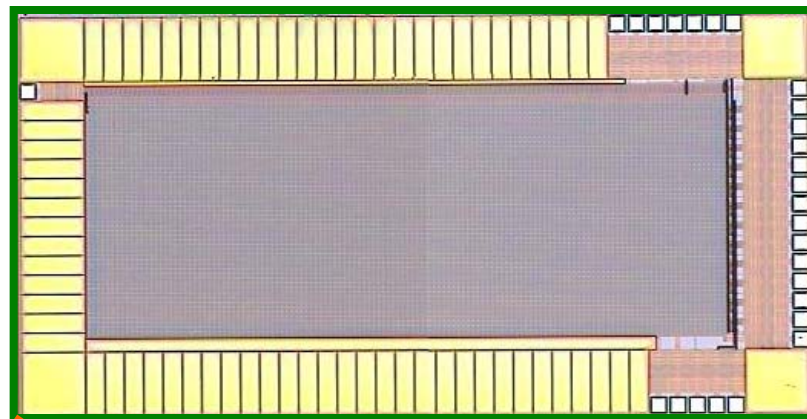
**all detectors (>15) function.**



# Example of Ease of Use



Pixel chip:  $132 \times 48 = 6336$  channels



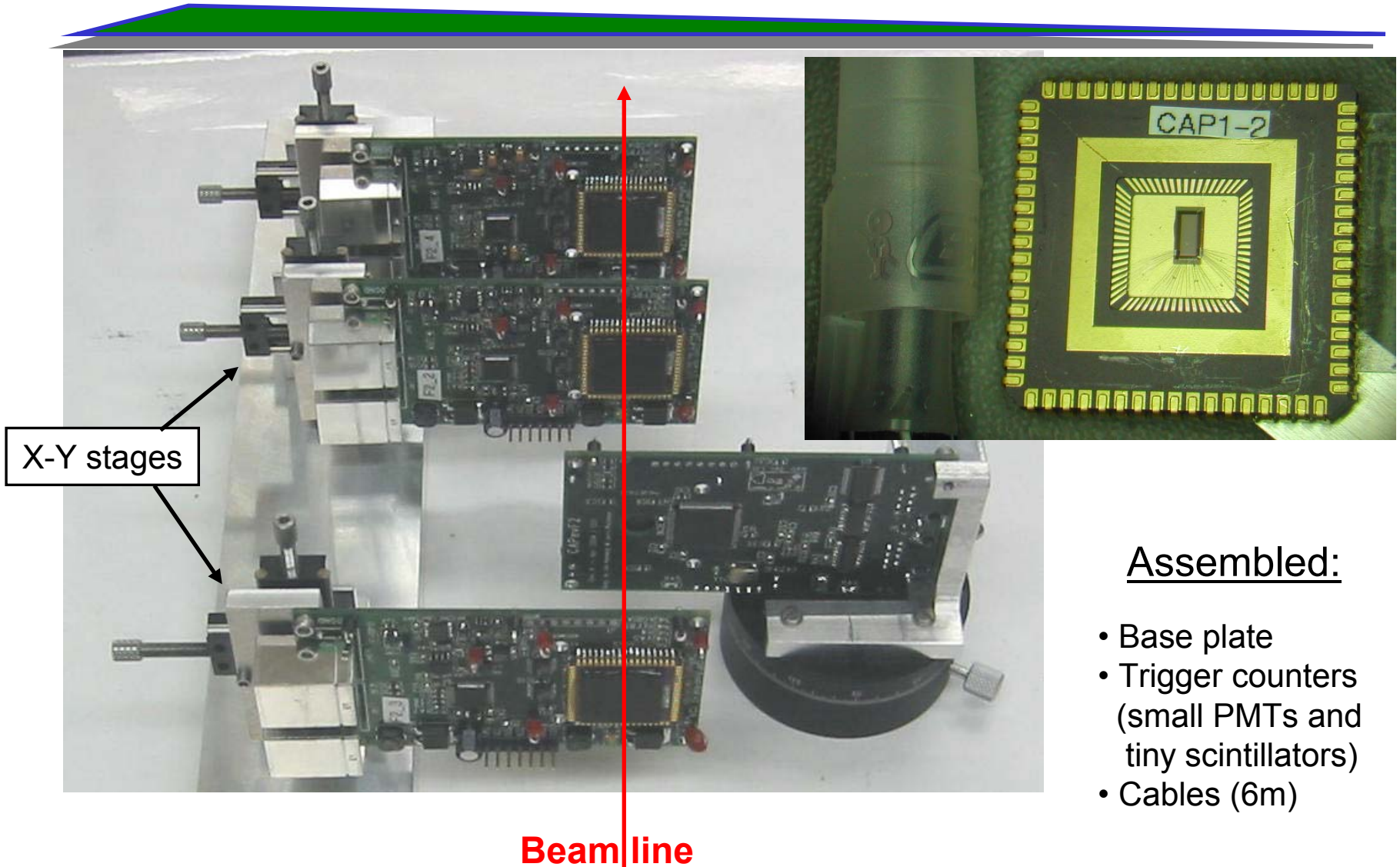
All LVDS digital I/O

300-600Mbaud link

~1mm x 3mm

On board ADC

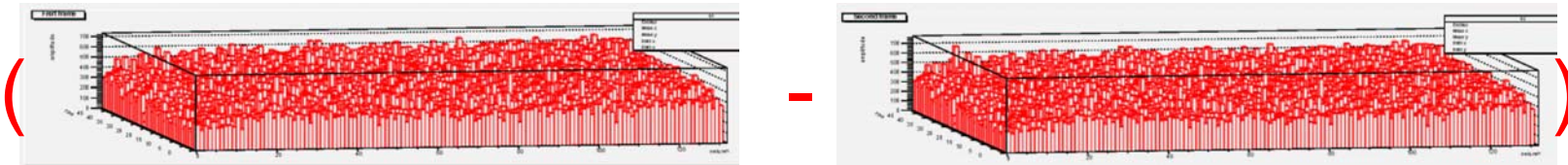
# Beam test bench



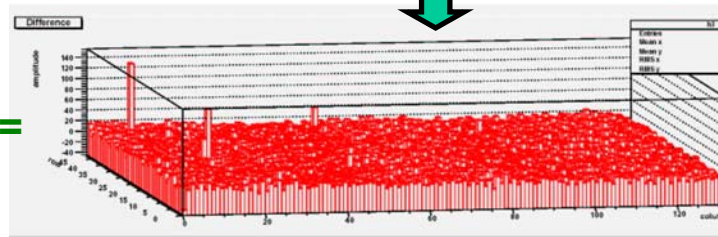
## Assembled:

- Base plate
- Trigger counters (small PMTs and tiny scintillators)
- Cables (6m)

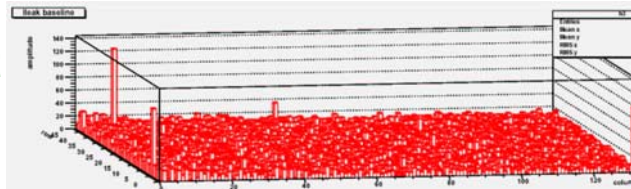
# Correlated Double Sampling (CDS)



Frame 1 - Frame 2 =



- Leakage current Correction

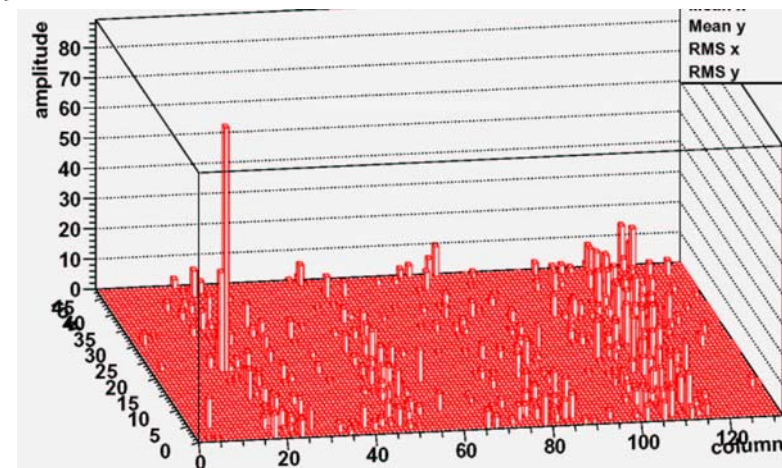


~fA leakage current (typ)  
~18fA for hottest pixel shown

**Hit candidate!**

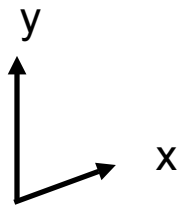
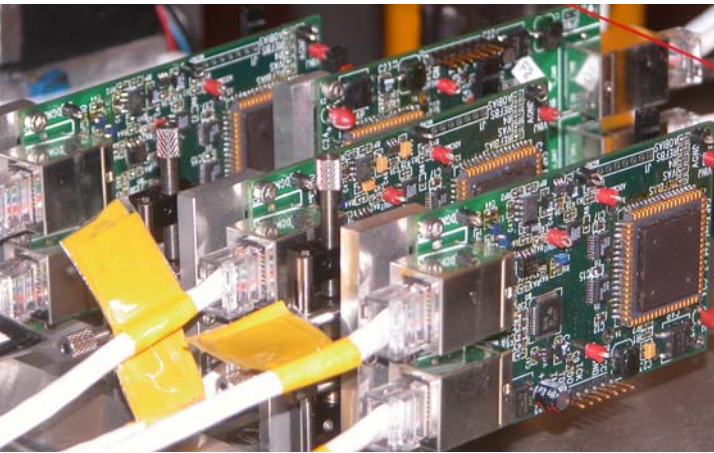
8ms integration

Can readout/process  
@ 20Hz ~ 16% live time (**CAP1!**)

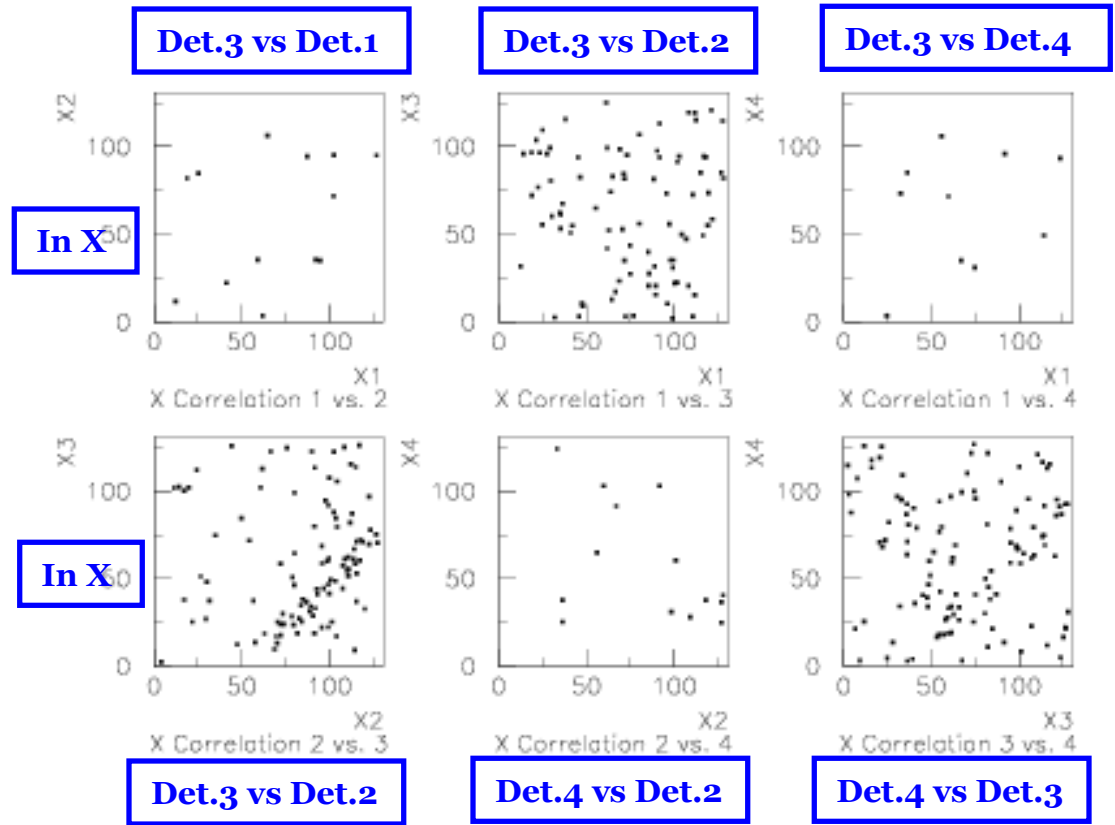


# Initial “by eye”

~1mm x 3mm “rice grain”



## Layer-by-layer correlations



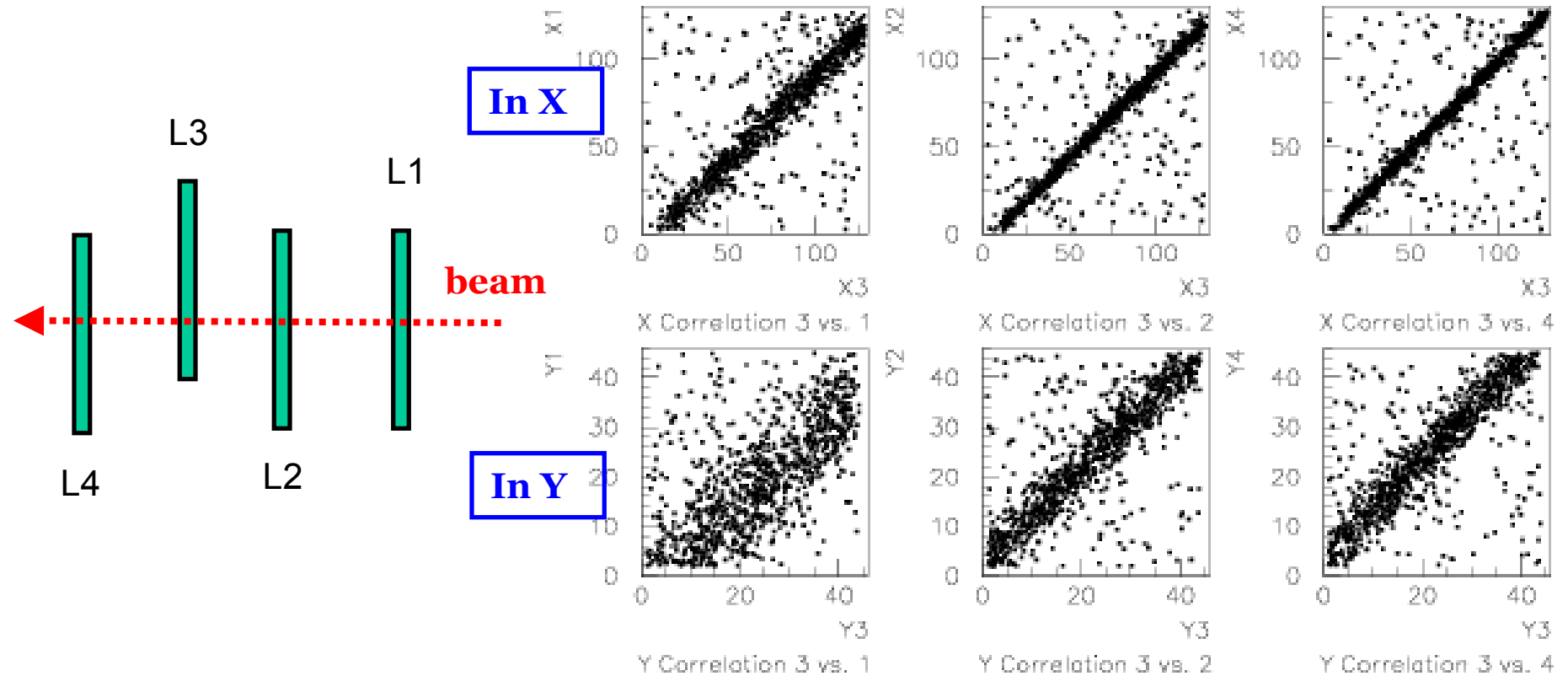
And after only 4 iterations...

# Improved Alignment

Det.3 vs Det.1

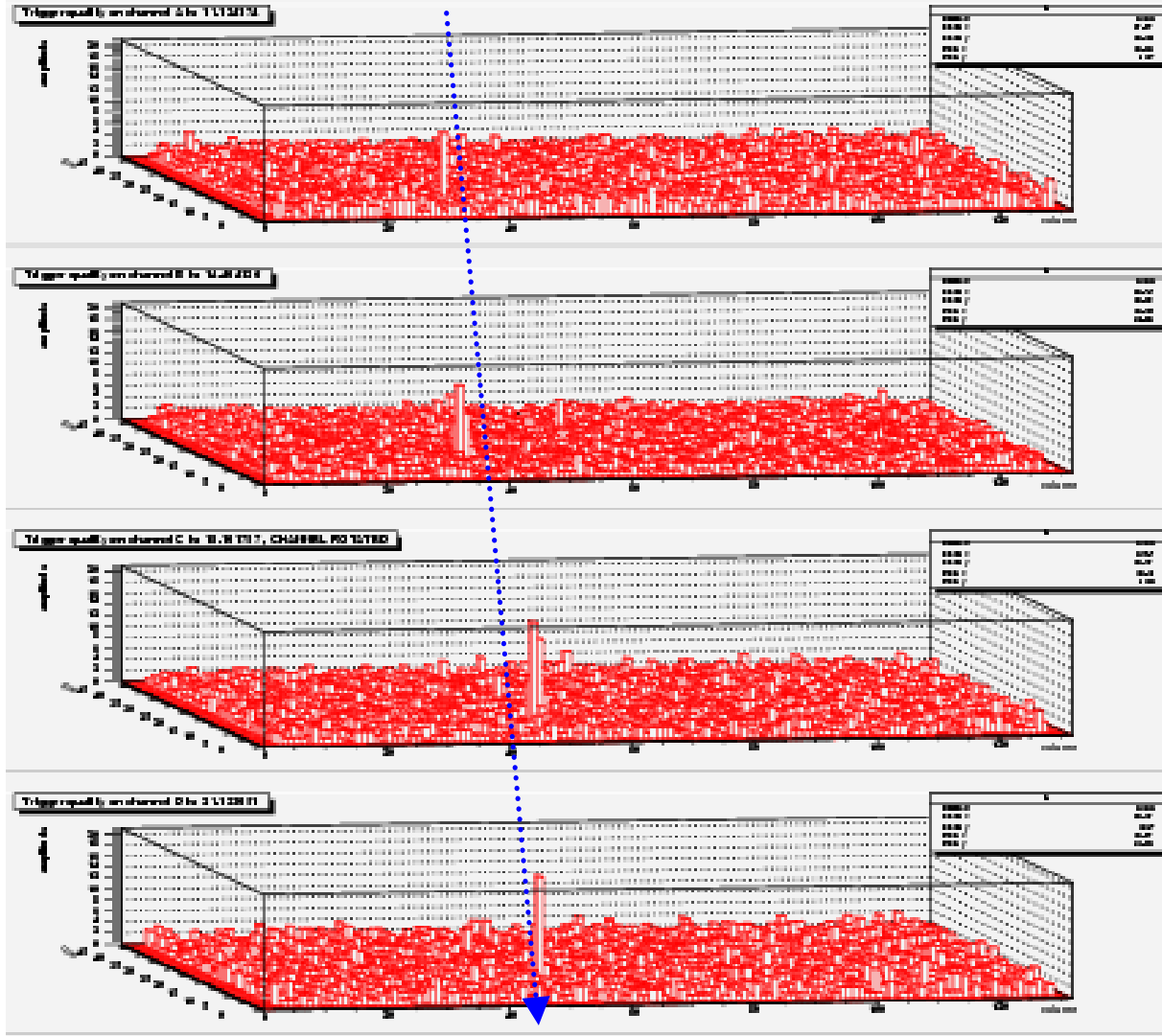
Det.3 vs Det.2

Det.3 vs Det.4

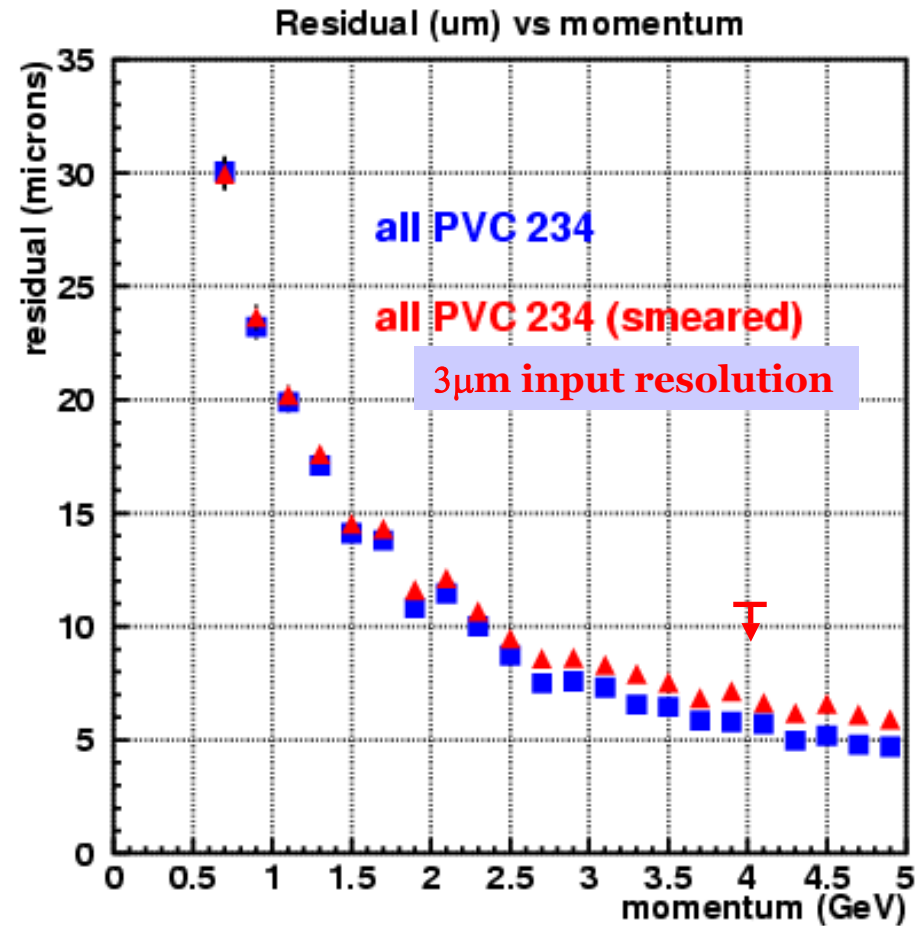
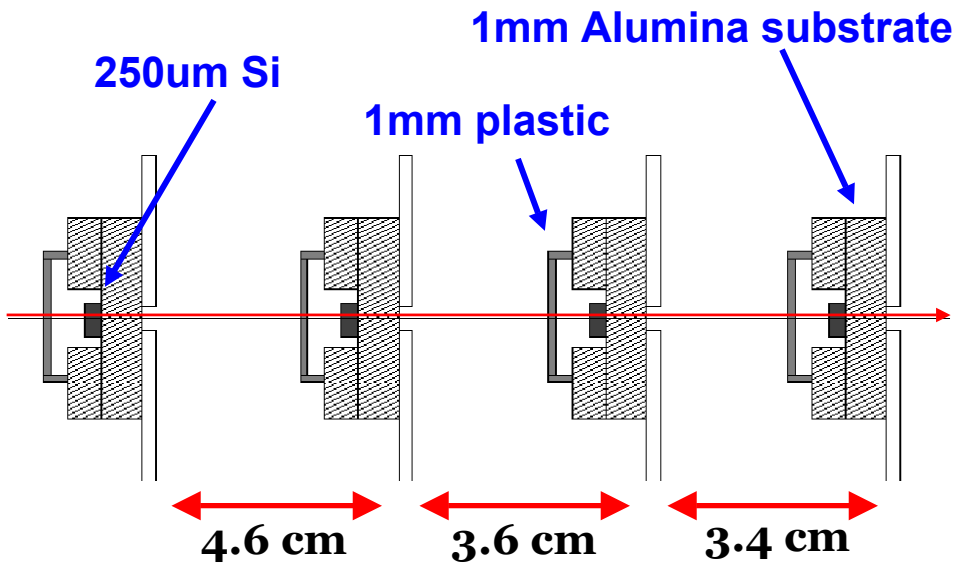


"online" plot

# Hits! alignment proof

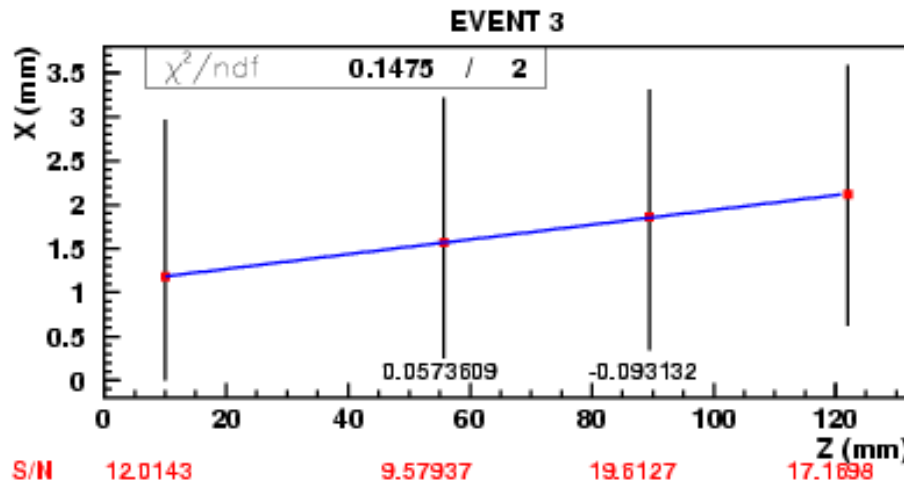


# Resolution: GEANT Expectation

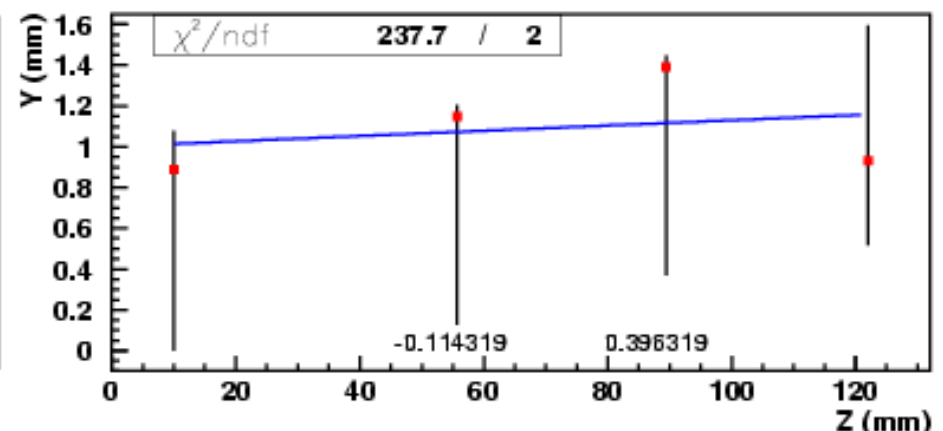
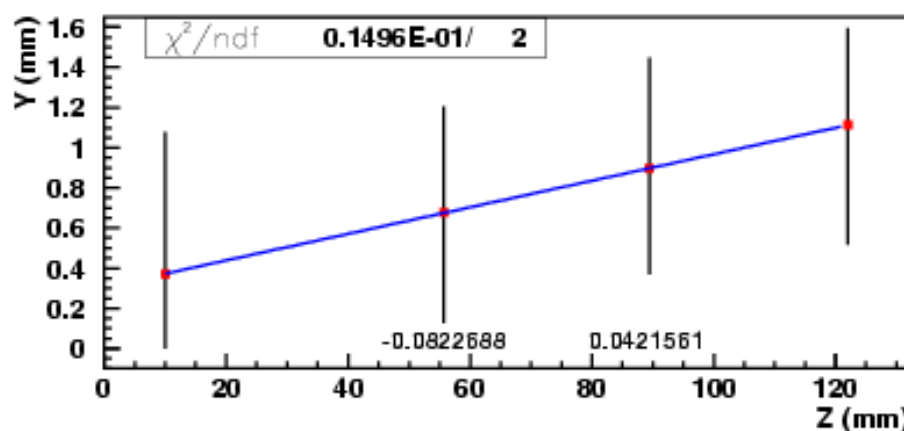
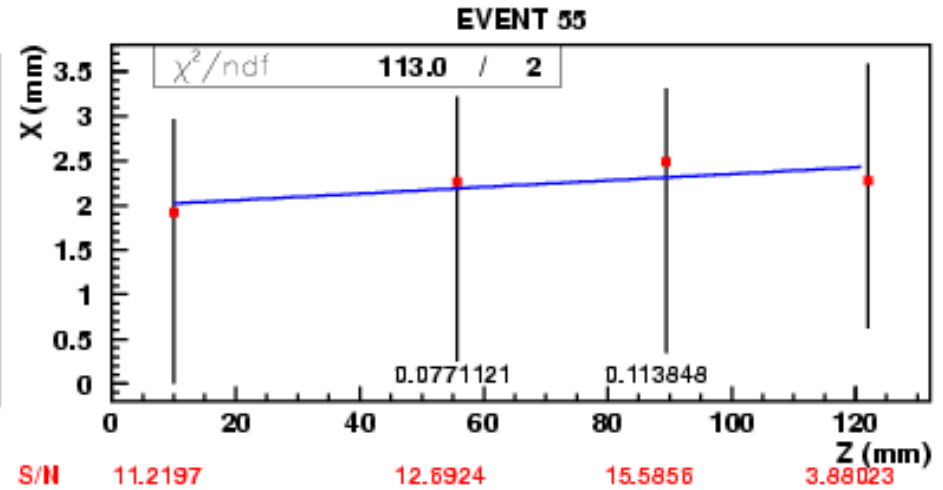


# Track Fitting / Residuals

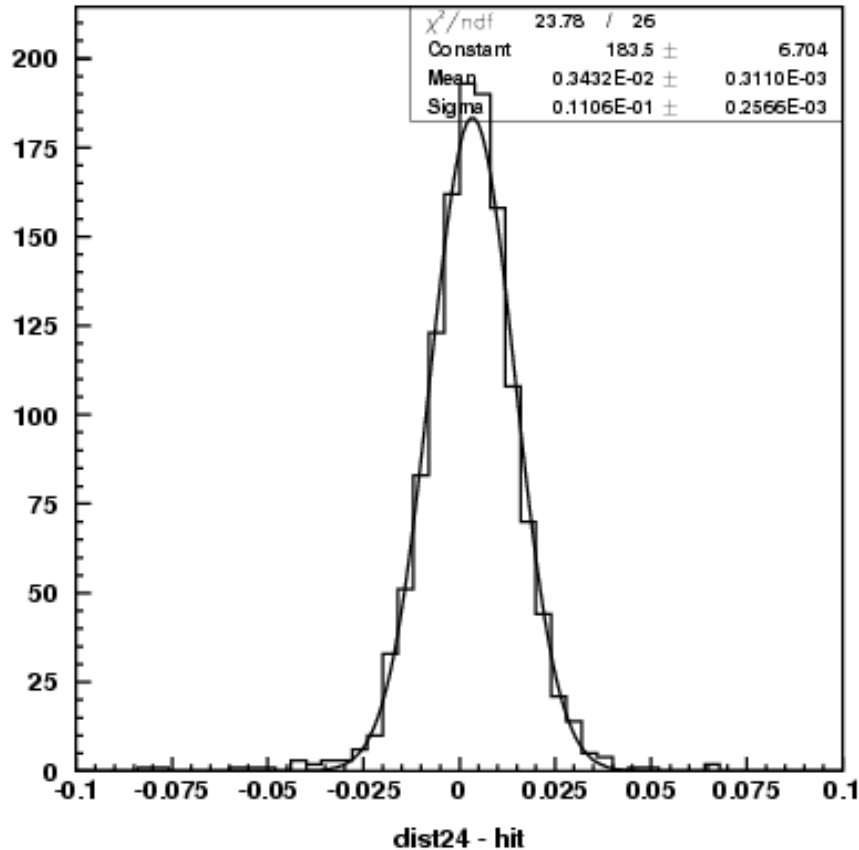
POUBELLE - Pixel Onscreen Utility for BELLE



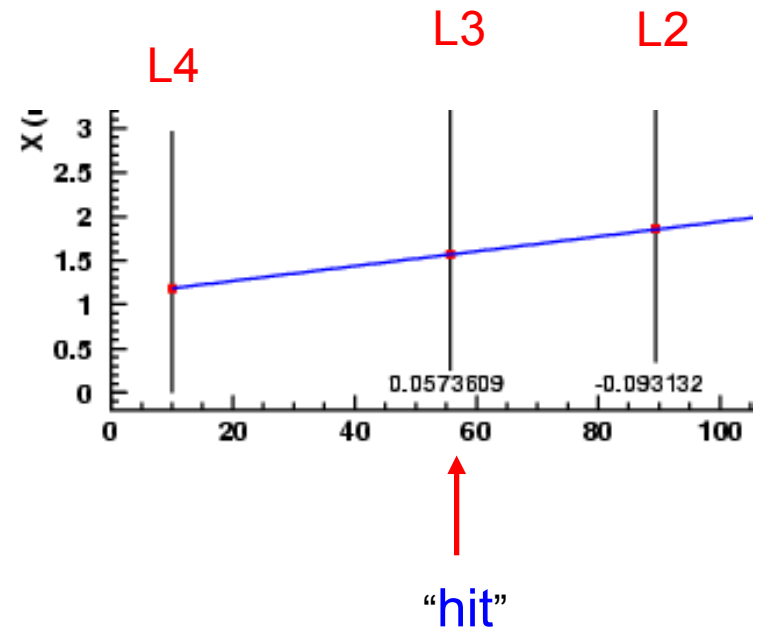
POUBELLE - Pixel Onscreen Utility for BELLE



# Resolution -- very preliminary



x-plane



Current Residuals:  
-11um in x plane  
-14um in y plane

# Critical R&D Items

## 1. Readout Speed

1. STAR phase 1, (x)LC OK(?), RAL efforts
2. Next R&D for Super B

## 2. Radiation Hardness

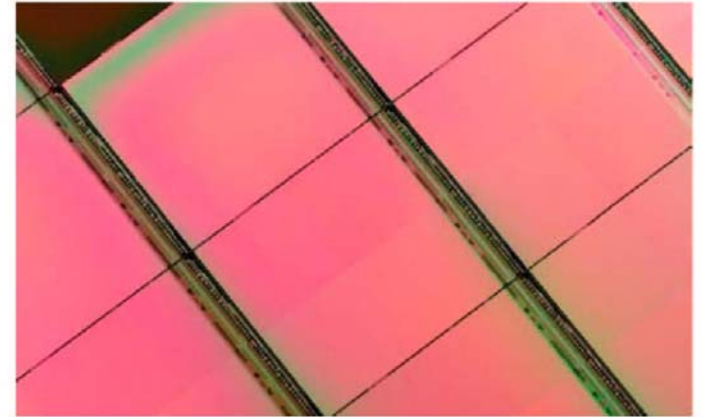
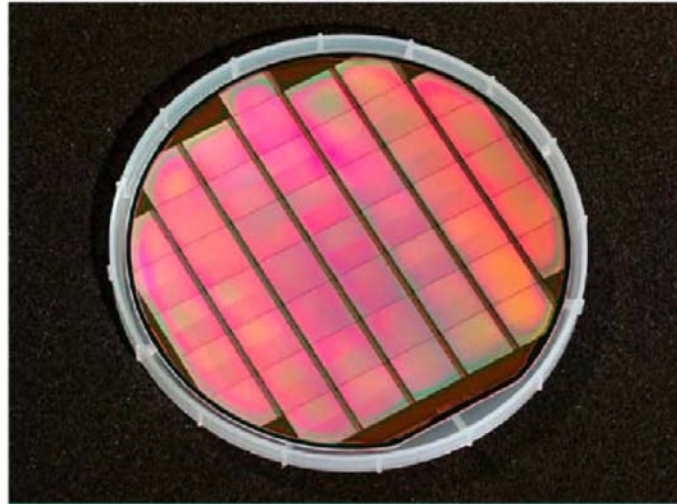
1. TESLA, STAR  $10^{12}$  n<sub>eq</sub>, >100kRad ionizing
2. Super-B: low E e<sup>-</sup>/γ CAP -- results shown next

## 3. Thin Detector - **LBNL**

## 4. Full-sized detector - **LEPSI**

# Critical R&D Items

## MAPS wafer scale prototype: Mimosa 5



### Mimosa-5 status

- 6 wafers delivered by AMS
- 3 wafer back-thinned (down to 120 $\mu$ m) and sliced
- prober tests of all wafers in progress: first estimation of yield ~30%
- beam tests at CERN: results as expected
- fine back-thinning tests at CNM Barcelona and ITE Warsaw

1. Rea

1. ST

2. No

2. Rad

1. ST

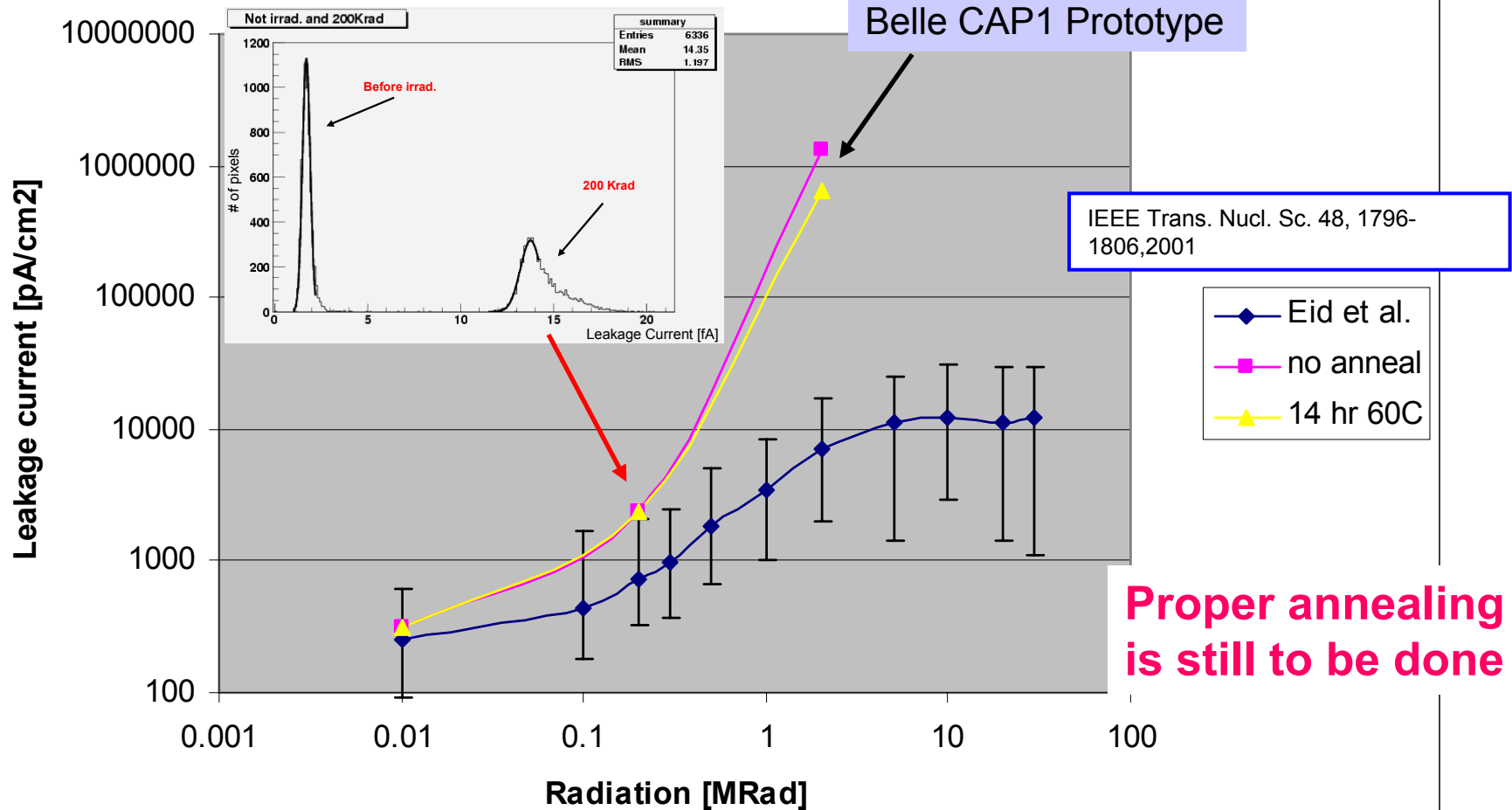
2. Su

3. Thi

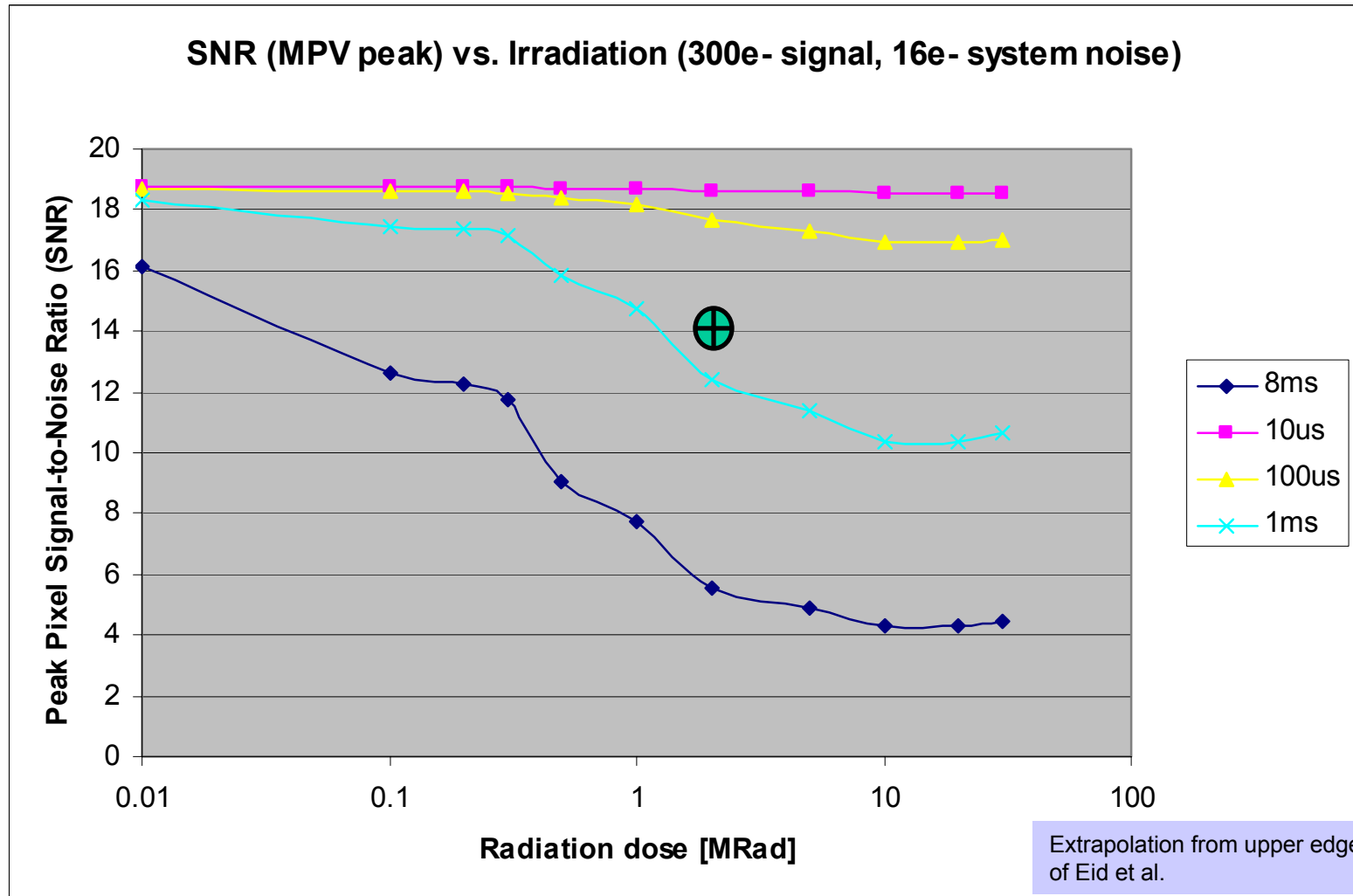
4. Full

# Irradiation leakage currents

## 0.35um CMOS APS Leakage Current



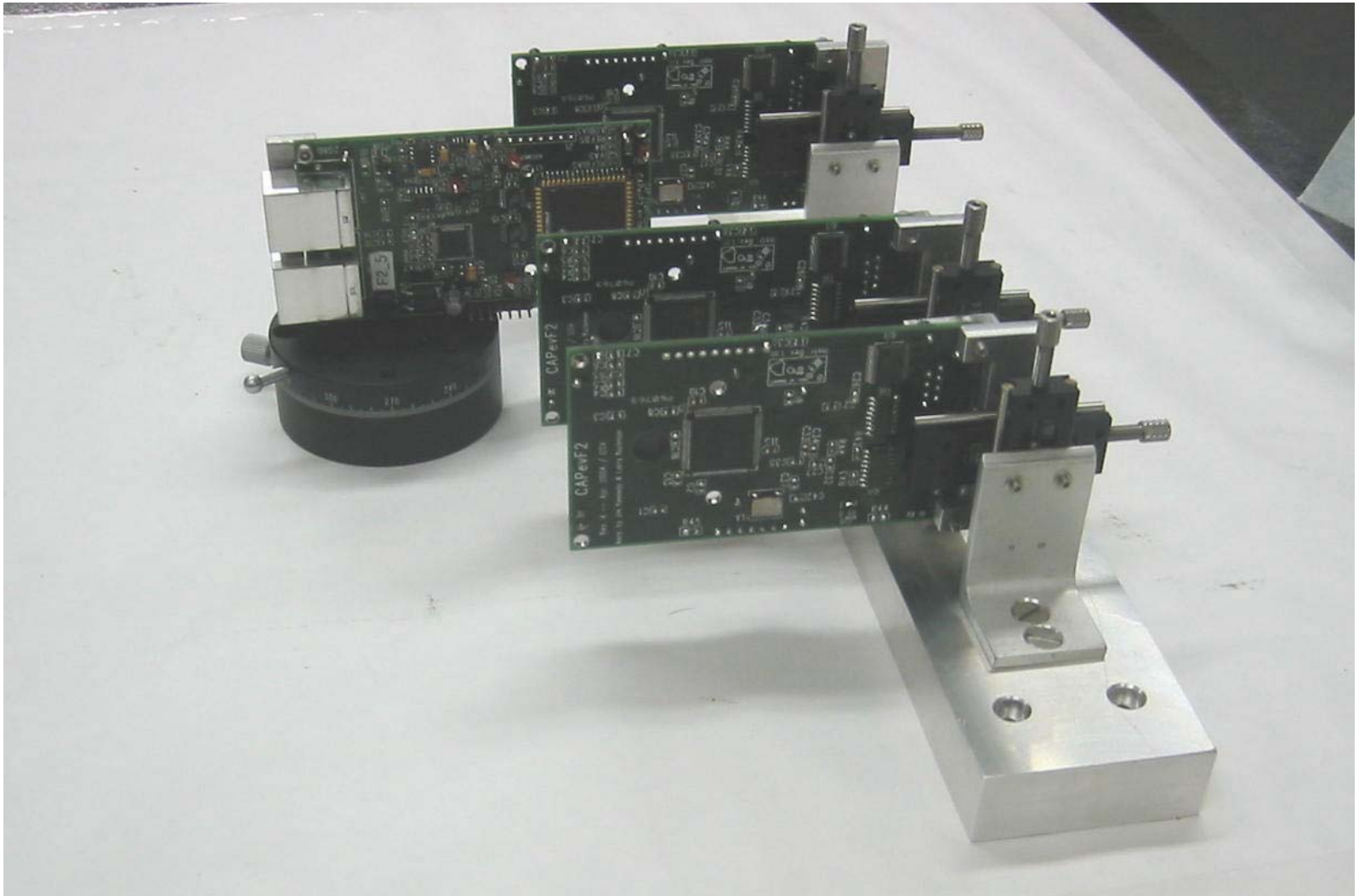
# MPV peak projections



# Composite Plans

- Full-sized detectors:
  - ENC degradation is large array  
(availability of stitching?)
  - Mechanics, power and cooling
- Data Handling (“The fire hose problem”)
  - High speed readout
  - On-chip sparsification/processing
- Further Radiation Damage Studies:
  - Demonstrate operation capability with highly irradiated detectors.  
(charge collection degradation)
- Precision dicing, handling and wire-bonding thin detectors

# Back up slides



# Required Transfer Rates

- CAP1 architecture (if  $10\mu\text{s}$  max. latency):

- 15mm radius:

- 67 Gpixels/s
- $\sim 1\text{Gpixel/s/pin}$

- 10mm radius

- 39 Gpixels/s
- $\sim 0.5\text{Gpixel/s/pin}$

Two ways around:  
- Multi-orbit  
- "Tiling"

- CAP2 architecture ( $\geq 100\mu\text{s}$  max. latency):

- 15mm radius:

- 6.7 Gpixels/s
- $\sim 100\text{Mpixel/s/pin}$

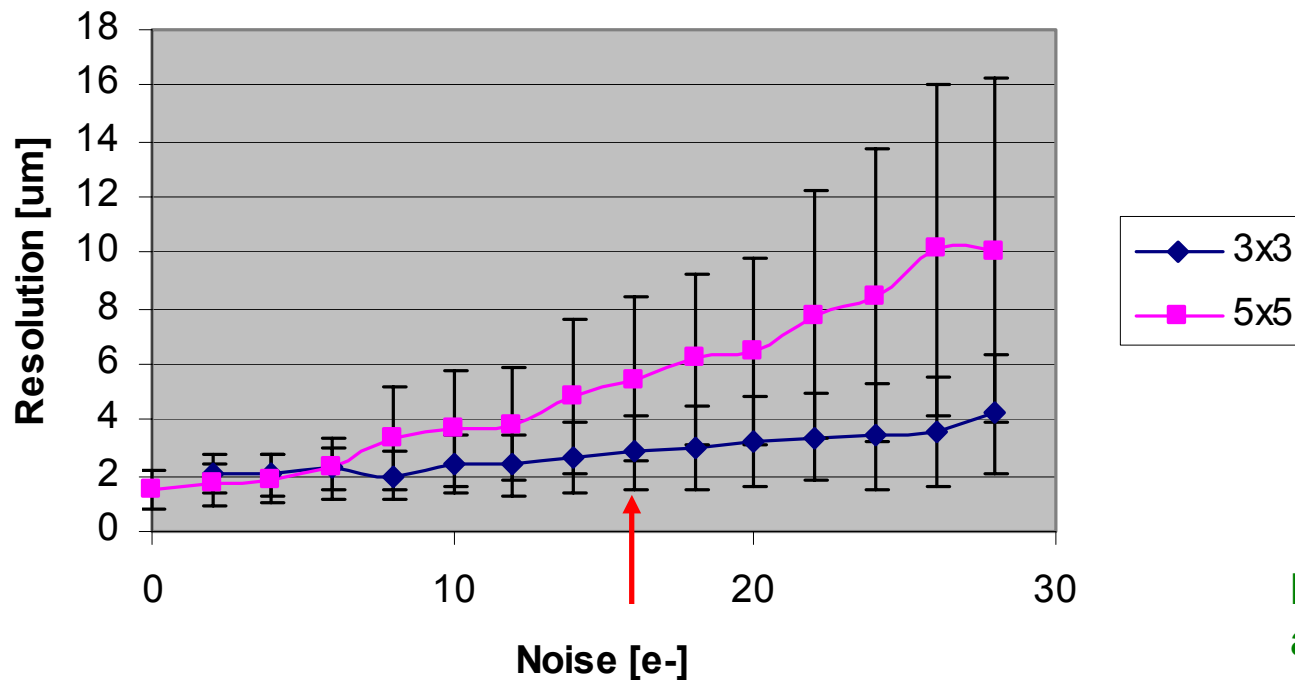
- 10mm radius

- 3.9 Gpixels/s
- $\sim 50\text{Mpixel/s/pin}$

Real max. latency  
Set by  $\langle L1/L2 \rangle$  rate

# Toy Monte Carlo

Noise Dependence



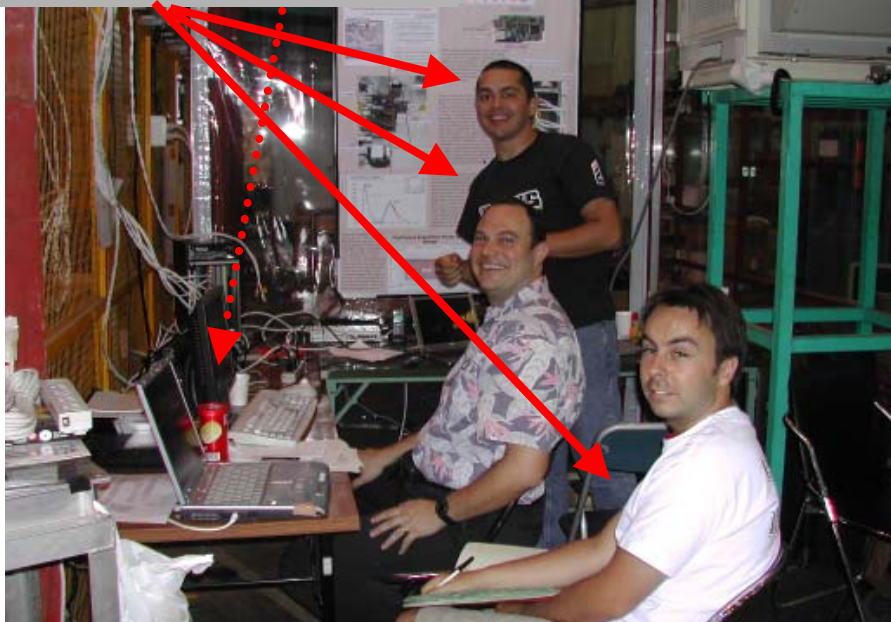
I got interested in the issue of Noise dependence

- random hits
- diffusion simulation:
  - substrate loss
  - recombination
  - add noise
- reconstruct track using c.o.g. and compare

Intrinsic could be as good as 3um:

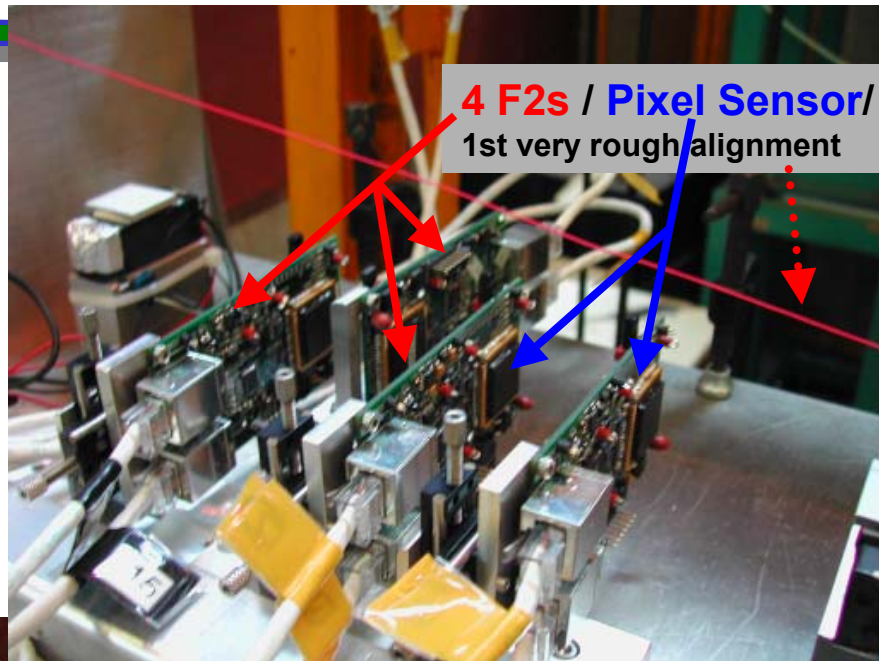
Alignment errors and multiple-scattering will likely dominate

**Shifters / chipsters**

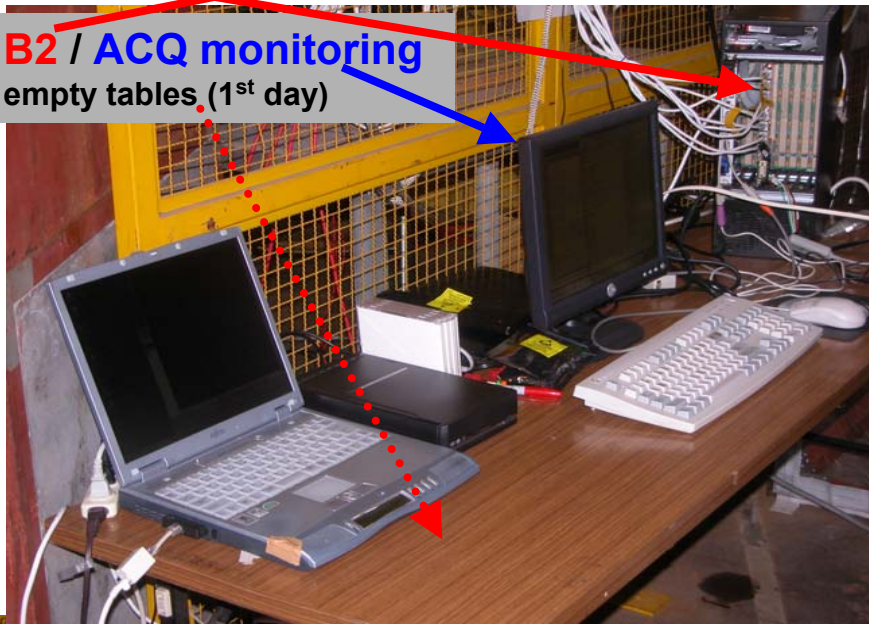


# Test Beam/ $\pi$ 2-area

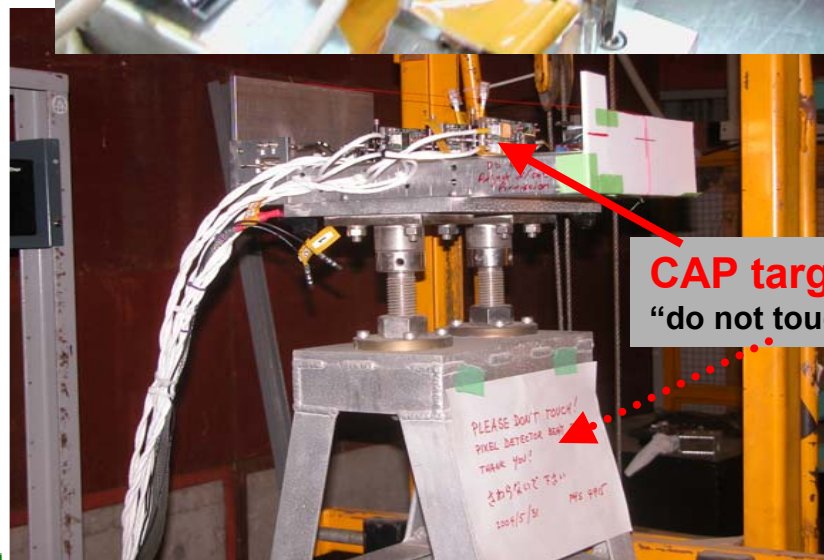
**4 F2s / Pixel Sensor / 1st very rough alignment**



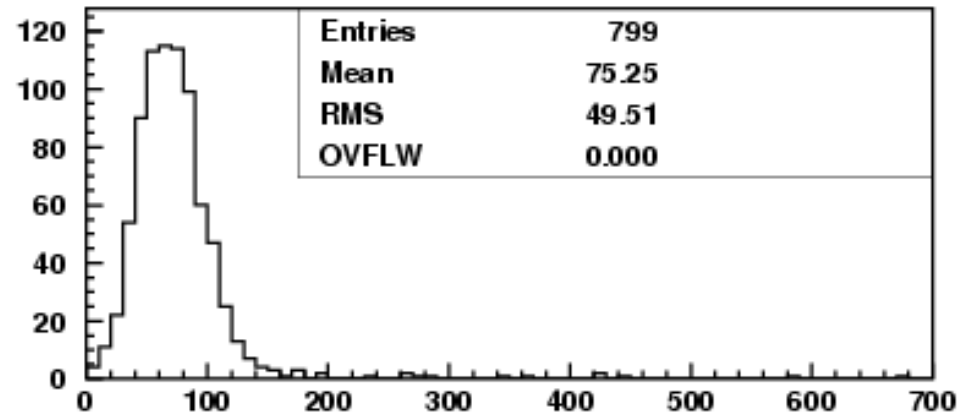
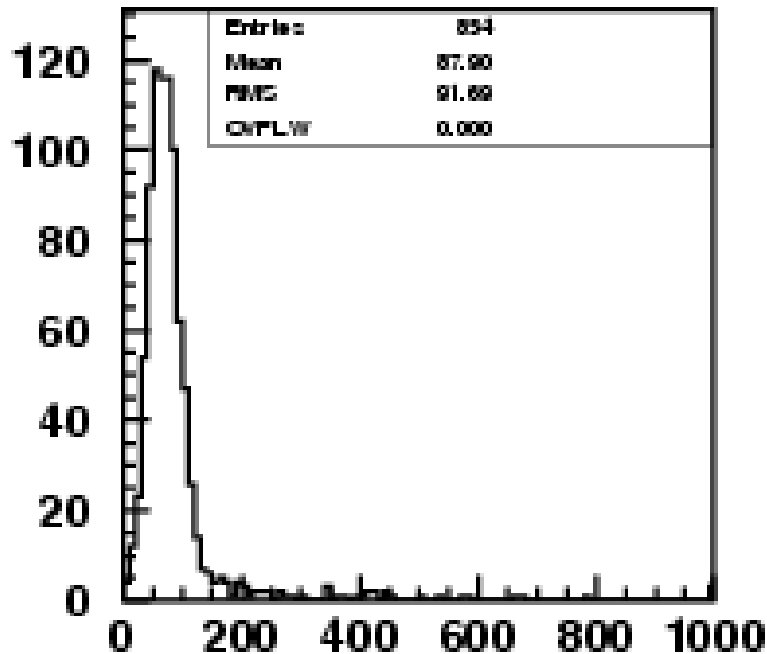
**B2 / ACQ monitoring empty tables (1<sup>st</sup> day)**



**CAP targets ! / "do not touch" sign**

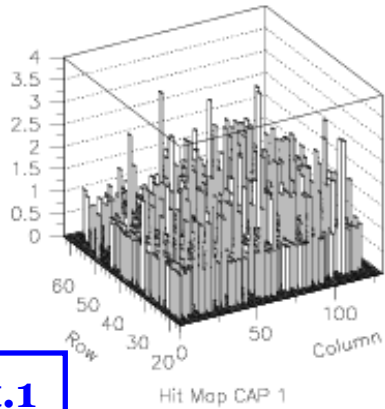


# Single Plane Efficiency

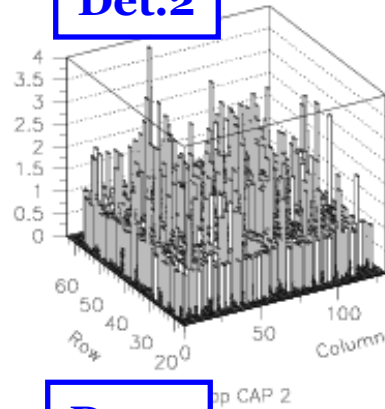


Preliminary:  $98.5 \pm 3.5\%$

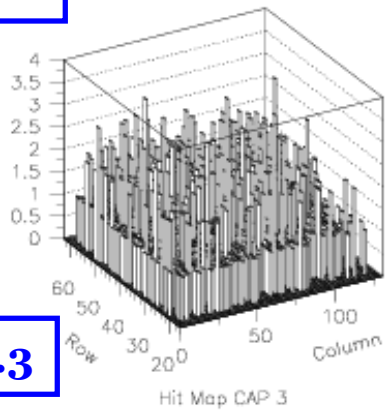
# Uniformity



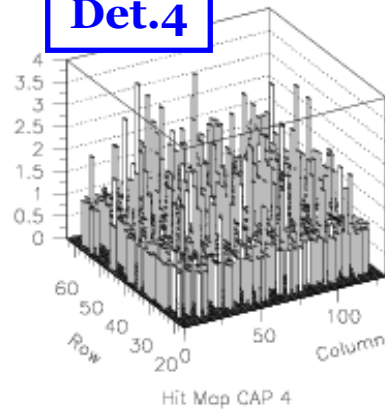
Det.1



Det.2

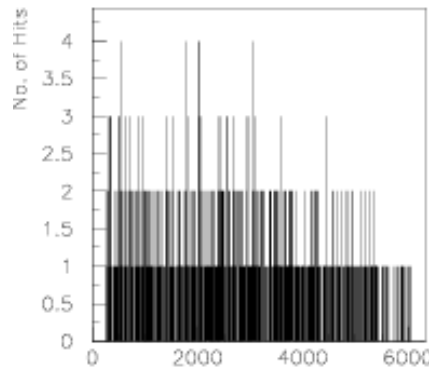


Det.3

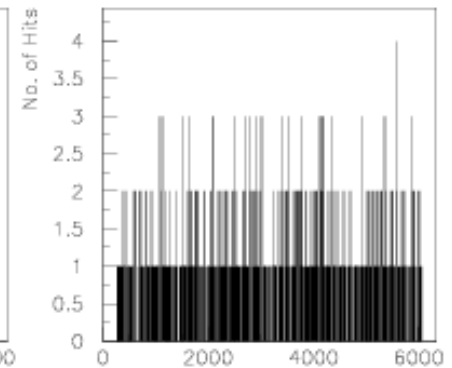


Det.4

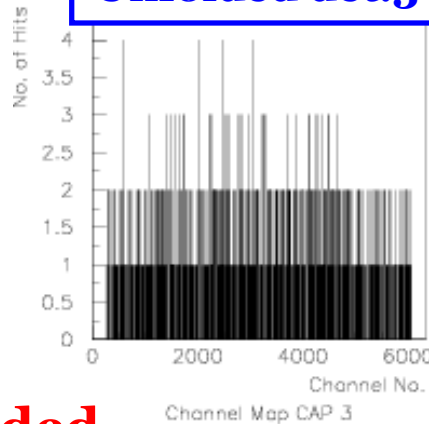
Unfolded det.1



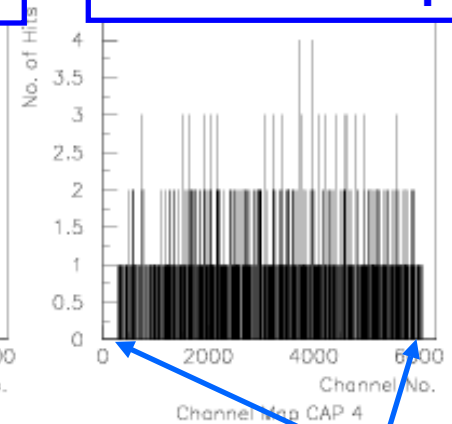
Unfolded det.2



Unfolded det.3



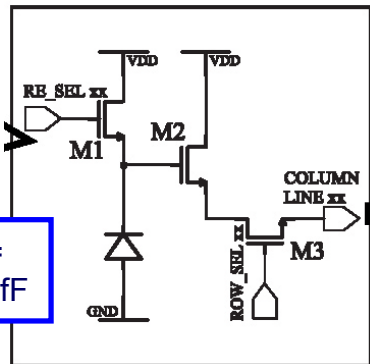
Unfolded det.4



**Less than 10 hot pixels excluded per layer: pixel yield >99%**

**Outer 2x rows/columns excluded**

# SNR Comparison



$C_{\text{extract}} = 3.2 \pm 0.6 \text{ fF}$

$50 \mu\text{V}/e^-$

Signal max.  
~ 560e-

Assuming 50%  
Signal collection  $\epsilon$   
In Max channel

60MSa/s possible

1.7x gain

$88 \mu\text{V}/e^-$

10-bit  
ADC

1mV/l**s**b

$11.3e^-/\text{l**s**b}$

Best in literature  
~10e- noise

~28e- noise  
(CM)

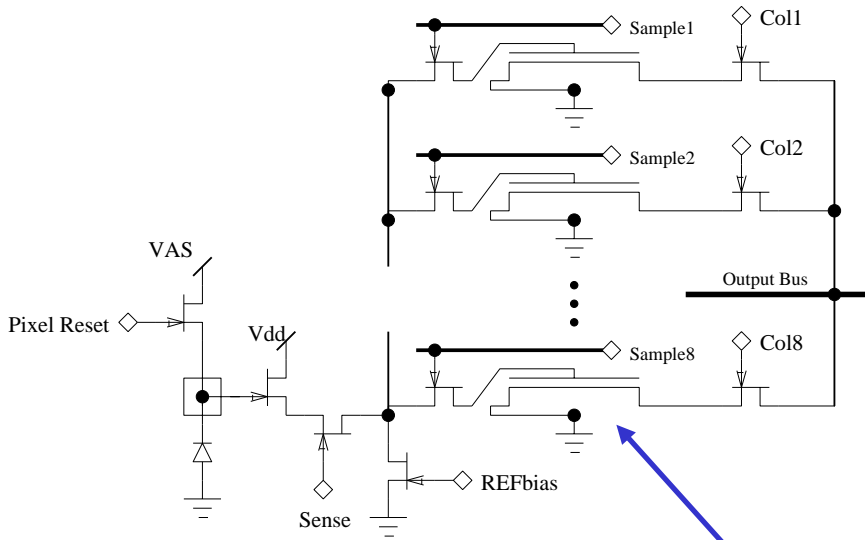
Even so,  
SNR ~ 20

SPICE extraction:	3.22 fF	+/- 0.6fF?	Detector:	14 $\mu\text{m}$	
Q=	1.60E-19 C/e-	Q=C*V	DSSD ref:	300 $\mu\text{m}$	24000 e-hole pair/m.l.p.
V=	4.97E-05 V/e-		Geom SF:	0.046667	
chip transfer: (SPICE)	0.78 Vout/Vin		Signal:	1120 e-	max produced
Resistive Divider:	1 was 2:1		Collection efficiency	0.5 w.a.g. -- in max channel	
CAPevF1 amp:	7 gain		Peak signal:	560 e-	
50 ohm series term:	0.5 voltage divide				
CAPevB1 amp:	0.65 gain				
<b>Net transfer gain:</b>	<b>1.7745</b>				
<b>Sensitivity:</b>	<b>0.088174 mV/e-</b>		<b>Expected SNR:</b>	<b>19.75096</b>	
CAPevB1 noise:	<b>2.5 ADC l<b>s</b>b noise</b>		<b>Sigma Set:</b>	7	
CAPevB1 ADC:	1 mV/l <b>s</b> b		<b>Threshold:</b>	60	
CAPevB1 sensitivity:	11.34122 e-/l <b>s</b> b		<b>m.l.p exp.</b>	49.37739	
CAPevB1 floor:	28.35306 e-				



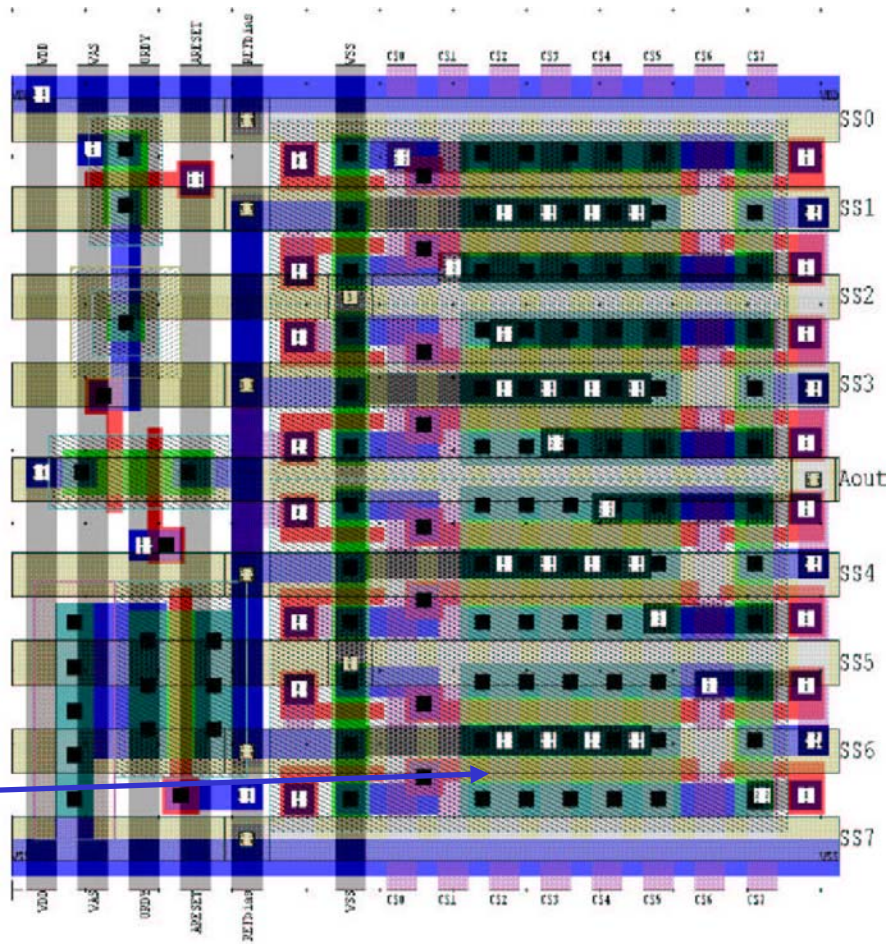
# Octal-pipeline (in $22.5\mu\text{m}^2$ pixel)

Yes!  
Random access, decoupled  
Read/Write

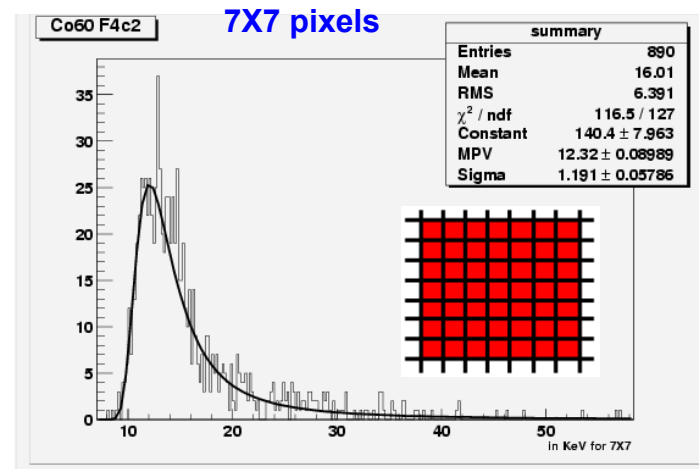
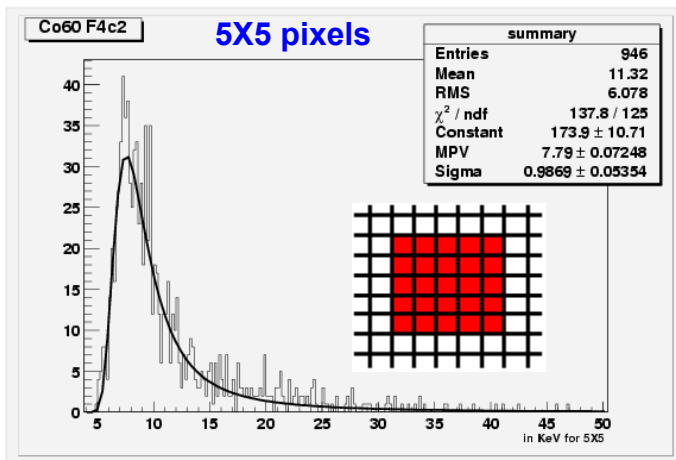
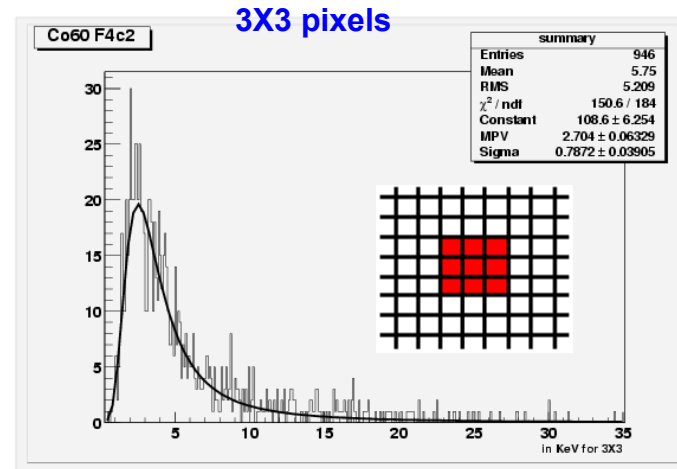
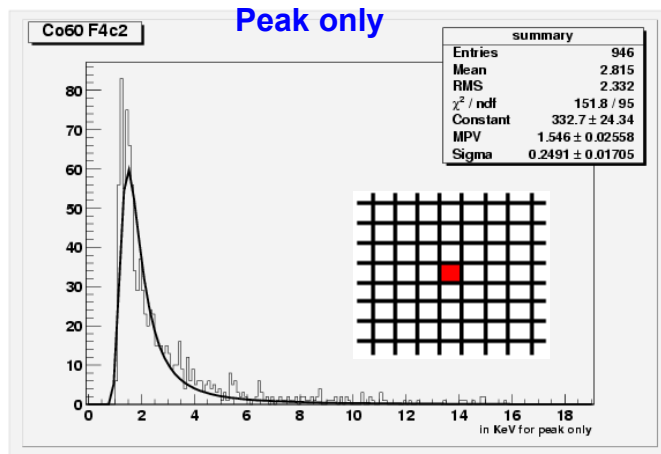


Storage cell

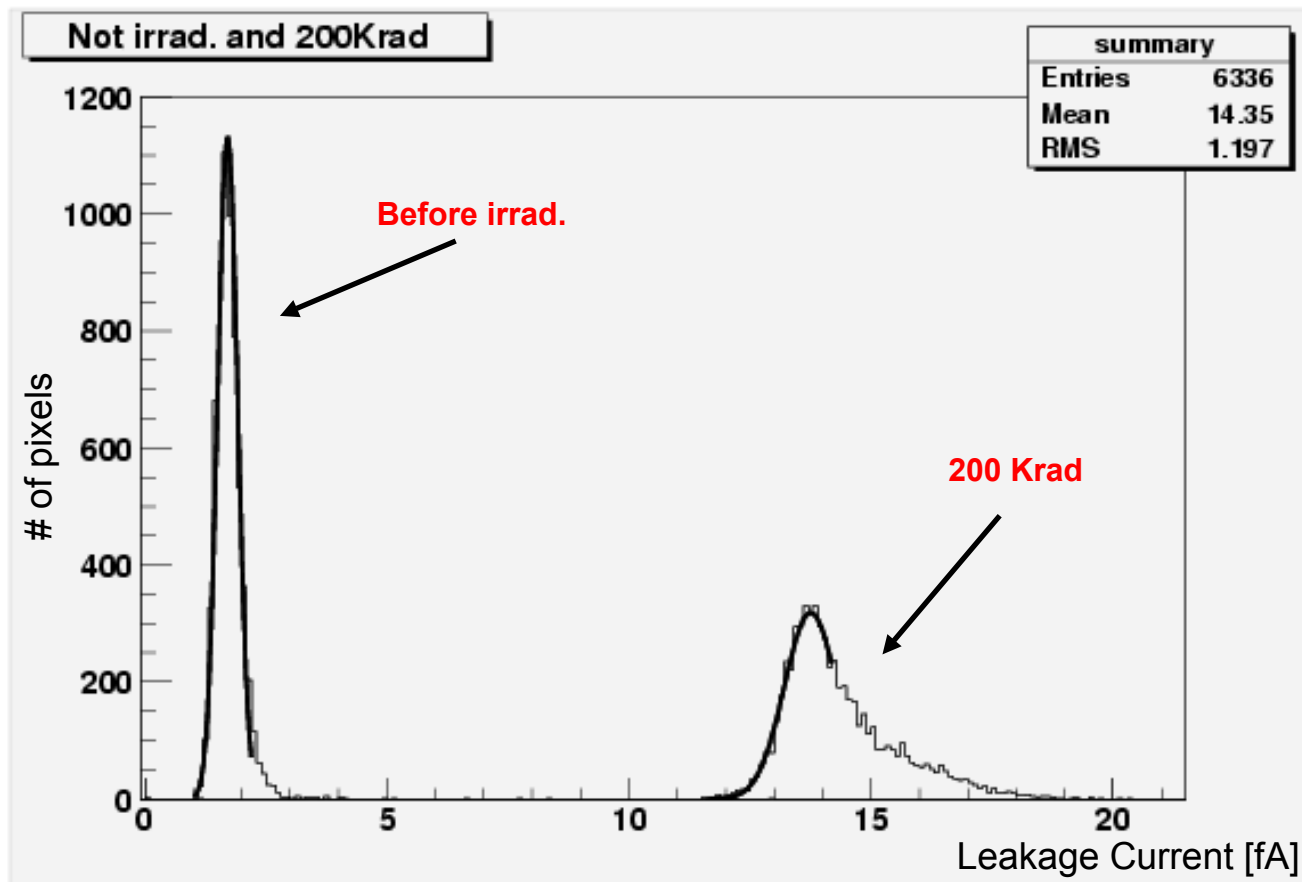
• 0.35 $\mu\text{m}$  Process 8x, more possible



# Charge Spread (pre-rad)



# Leakage Current (cont.)



# MIMOSA History

**MIMOSA = Minimum Ionising MOS Active pixel sensor**

Prototype	Process	Epi-thickness	Pixels/array	Pitch	Max. Clock	Peculiarity
<b>MIMOSA1</b>	AMS 0.6 $\mu\text{m}$	14 $\mu\text{m}$	64x64	20 $\mu\text{m}$	5 MHz	Thick epitaxy Technology demo.
<b>MIMOSA2</b>	MIETEC 0.35 $\mu\text{m}$	4.2 $\mu\text{m}$	64x64	20 $\mu\text{m}$	25 MHz	Thin epitaxy Noise studies
<b>MIMOSA3</b>	IBM 0.25 $\mu\text{m}$	2 $\mu\text{m}$	128x128	8 $\mu\text{m}$	40 MHz	Deep-sub $\mu\text{m}$ process – rad. hard.
<b>MIMOSA4</b>	AMS 0.35 $\mu\text{m}$	0 !!!	64x64	20 $\mu\text{m}$	40 MHz	Low doping substrate
<b>MIMOSA5</b>	AMS 0.6 $\mu\text{m}$	14 $\mu\text{m}$	1020x1024	17 $\mu\text{m}$	40 MHz	Real scale sensor
<b>MIMOSA6</b>	MIETEC 0.35 $\mu\text{m}$	4.2 $\mu\text{m}$	30x128	28 $\mu\text{m}$	30 MHz	CP read-out int. functionalities