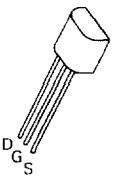
N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN3306A

ISSUE 2 - MARCH 94

FEATURES

* 60 Volt V_{DS}
* $R_{DS(on)}$=5Ω



E-Line
TO92 Compatible

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	60	V
Continuous Drain Current at T_{amb}=25°C	I_D	270	mA
Pulsed Drain Current	I_{DM}	3	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	625	mW
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	60		V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.8	2.4	V	I_D=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		20	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		0.5 50	µA µA	V_{DS}=60V, V_{GS}=0 V_{DS}=48V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	750		mA	V_{DS}=18V, V_{GS}=10V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		5	Ω	V_{GS}=10V,I_D=500mA
Forward Transconductance(1)(2)	g_{fs}	150		mS	V_{DS}=18V,I_D=500mA
Input Capacitance (2)	C_{iss}		35	pF	V_{DS}=18V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		25	pF	
Reverse Transfer Capacitance (2)	C_{rss}		8	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		5	ns	V_{DD}≈18V, I_D=500mA
Rise Time (2)(3)	t_r		7	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		6	ns	
Fall Time (2)(3)	t_f		8	ns	

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2%
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator

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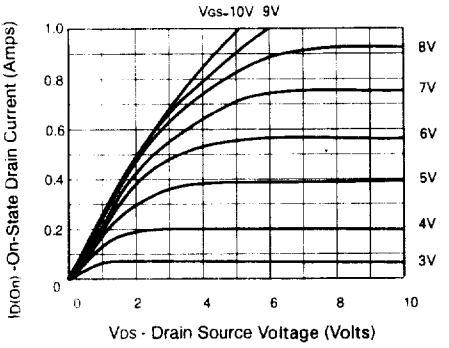
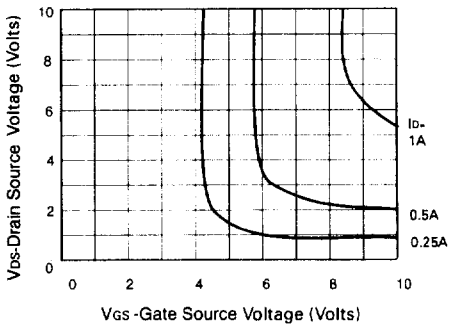
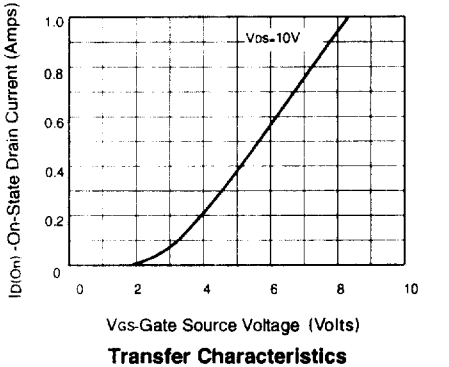
TYPICAL CHARACTERISTICS



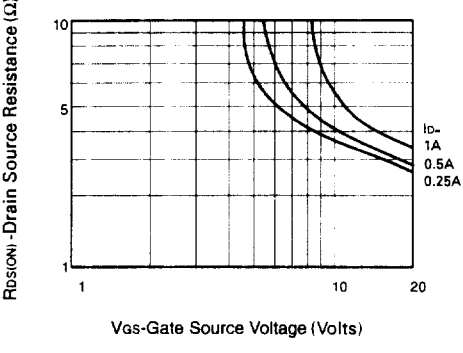
Saturation Characteristics



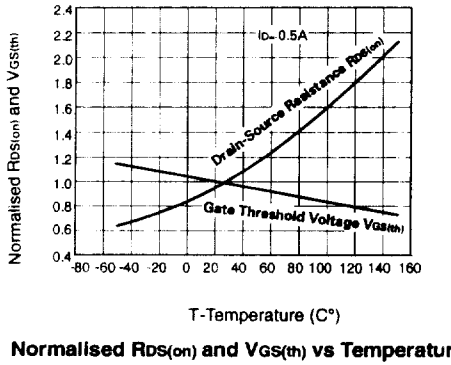
Voltage Saturation Characteristics



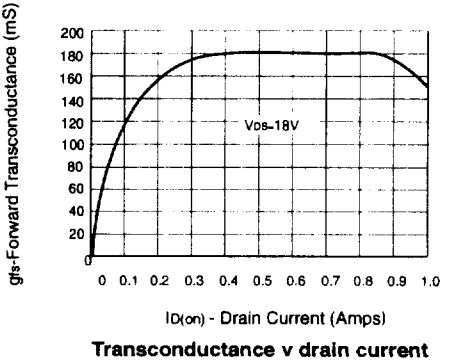
Transfer Characteristics



On-resistance vs gate-source voltage

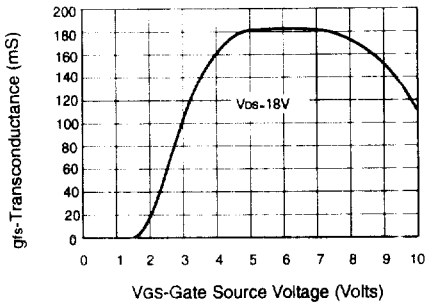


Normalised RDS(on) and VGS(th) vs Temperature

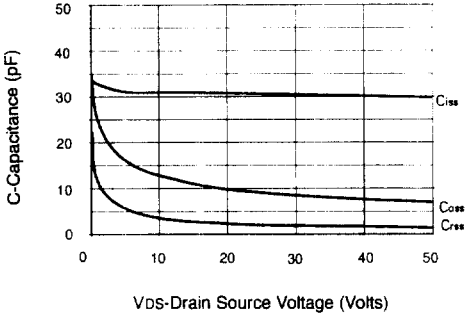


Transconductance v drain current

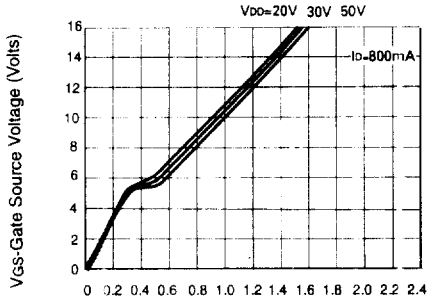
TYPICAL CHARACTERISTICS



Transconductance v gate-source voltage



Capacitance v drain-source voltage



Gate charge v gate-source voltage